REPORT

NAVAL POSTGRADUATE SCHOOL

Monterey, California

THESIS

APPLICATION OF CHARGE COUPLED DEVICES FOR INFRARED SIGNAL PROCESSING ON THE FOCAL PLANE

by

Kurt Alfred Pfennig

Thesis Advisor: Tien Fan Tao

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analyzed with emphasis on the bandlimiting mechanism in the surface equilibration input method. Furthermore, ideas for signal processing in the IR focal plane are discussed, such as the frame to frame subtraction, moving target detection and convolutional scanning.

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I. INTRODUCTION

Charge Coupled Devices (CCD) have provided compact, high resolution, low light level image sensors with a theoretical limit of operation at very low charge levels with a few electrons (about 10 at starlight) in a single charge packet, particularly, if a cooled device is used[1]. CCDs for image sensing and focal plane signal processing in the infrared (IR) region are still at the beginning stage of the development.

With today's large scale integration (LSI) technology, an effort to combine IR sensors and CCD signal processing devices directly to a focal plane processing unit is underway.

In the far IR region, corresponding to target temperatures around 300K, where maximum contrast occurs, the problem to discriminate against high background level needs further research in CCD technology for combinations of silicon CCDs and detector materials. Efforts are being made to identify the properties of the interfaces between insulators and several well known IR sensitive materials, for example, to develop a high yield fabrication process, to integrate mercury cadmium telluride detectors with silicon CCD shift registers or CCD processing units. CCDs have proved their quality as low noise, small size, and low power consumption devices suitably applicable as processing units in conventional electronic circuits; analog delay, time delay and integration, analog matched filters, transversal filters, convolvers, adders, multipliers using split gate technology, and memories.

In addition to the long wavelength IR region, the second generation of forward looking infrared (FLIR) imagers are also interested in the near and middle IR region, for example, the focal plane arrays of about 1000 detectors made of lead selenide telluride (PbSeTe) on silicon CCD substrate. Other detector materials for the 1-5 micron region are lead sulfide (PbS) and lead selenide (PbSe). All these materials need only be cooled to 200K, where light weight thermoelectric coolers simplify the cooling requirements[2]. Short wavelength sensors are useful in applications where targets of temperatures above 500K are to be detected; for example, in space surveillance: tail pipes or plumes of a jet aircraft, burning booster propellants of large intercontinental missiles or launches of small missiles.

The technology for IR imagers can be separated into two categories:

* The Monolithic Approach
* The Hybrid Approach.

The monolithic approach for IR focal plane arrays can further be subdivided into arrays using extrinsic silicon doped with materials which stretches the intrinsic cutoff frequency of about 1 micron into the middle IR region, and intrinsic semiconductor arrays made of well known detector materials, such as indium antimonide (InSb), mercury cadmium telluride, and lead-tin telluride. The disadvantage of these sensor materials lies in their low operating temperature of 25K to 60K for extrinsic and 60K to 100K for intrinsic semiconductors. Furthermore, the technology for these exctic materials is not as well established as for silicon.

In the hybrid approach, non-silicon detectors or polycrystalline film detectors such as PbS and PbSe are

integrated on a silicon substrate, containing preamplifier, CCD or even more sophisticated focal plane processing units to be developed in the future.

In this thesis, a hybrid IR imager is studied. An array of non-silicon infrared detectors, such as the PbS and PbSe are integrated and ac coupled to a CCD processing array, which is designed to process a signal gain. In Chapter II, an ac-coupling interface circuit providing the necessary low-pass filter characteristic for a sampled data device is designed for on-chip fabrication. Ac-coupling is particularly advantageous for IR imagers to achieve background suppression and to avoid fixed pattern noise arising from sensor arrays and bias components. Chapter III studies quantitatively the unique feature of a signal voltage gain in a CCD delay line. The static transfer characteristic of a CCD with a special input stage design is analysed. The overall gain factor for a CCD is predicted and experimentally verified. This gain mode of operation provides the possibility to process a signal gain while the detector signal is read out of an array. Thus the preamplifier usually necessary in the interface circuit can be eliminated. In Chapter IV, different noise contributions arising in the CCD are analysed. Noise contributions from the input stage is of mayor concern in a hybrid IR imager, using the CCD as a preamplifier. Proper interface of the CCD preamplifier with the IR sensor is studied for sensor limited or background limited operations. Chapter V describes some ideas of signal processing on IR focal plane where processing both in the spatial and in the transform domains will be discussed separately.

II. IR-DETECTOR AND CCD-AMPLIFIER INTERFACE

A. INTRODUCTION

The interface circuit between a photoconductive IR detector and the input stage of a CCD operating in a high gain mode will be analysed. This combination of a single detector and a CCD processor could be a part of a focal plane image processor.

B. INTERFACE DESIGN OBJECTIVES

The interface circuit, coupling the detector signal to the CCD should meet the following objectives:

1. All circuit elements must be integrated with the IR detectors and the SiCCD on the same chip.
2. Appropriate detector bias condition must be maintained under intermediate temperature operation (200K).
3. The frequency response should have bandpass characteristic with low frequency corner down to 1 Hz or less and upper frequency roll-off at about 10 KHz to bandlimit the white noise from detector and bias resistor.
4. Element to element nonuniformities which are unavoidable during the fabrication process of a focal plane array, resulting in "fixed pattern " noise, must be minimized.
5. The insertion loss is to be kept at a minimum value, since no active device will be considered for the interface circuit.

6. The dc-bias condition for the CCD input must be maintained.

C. INTERFACE REALIZATION

For efficient readout of the detector signal the load resistor and the detector are matched. Therefore, PbSe or Pb detectors at 200K require bias resistors of about 1-10 megaohms. To meet objective one and two, the only integrated circuit resistor giving this high resistance is the depletion MOSFET resistor. It is estimated, that a total capacitance of about 1-2 pF is associated with the detectors and the electrical connecting paths on the chip, leaving the bias resistor value as the only parameter which could be varied in design. However, maximum allowable power dissipation of the detector, RC time constant in the input circuit, and the very high input impedance of the CCD preamplifier dictate a value of the bias resistance in the order of the detector resistance.

Objectives three and four are met by using straightforward RC filtering and ac-coupling techniques. However, the selection of the coupling capacitance must satisfy two requirements. First, the signal must be effectively transferred to the CCD. Since the CCD input capacitance is in the order of 0.2pF, the coupling capacitance must be several times higher. In this study, a value of 2pF is selected. Second, it cannot be made bigger because its size cannot exceed the space allowed by optical design considerations. Signals, arising from the background flux of the earth, are represented as a dc voltage at the detector output, since this flux varies only diurnal or seasonal with the solar radiation.

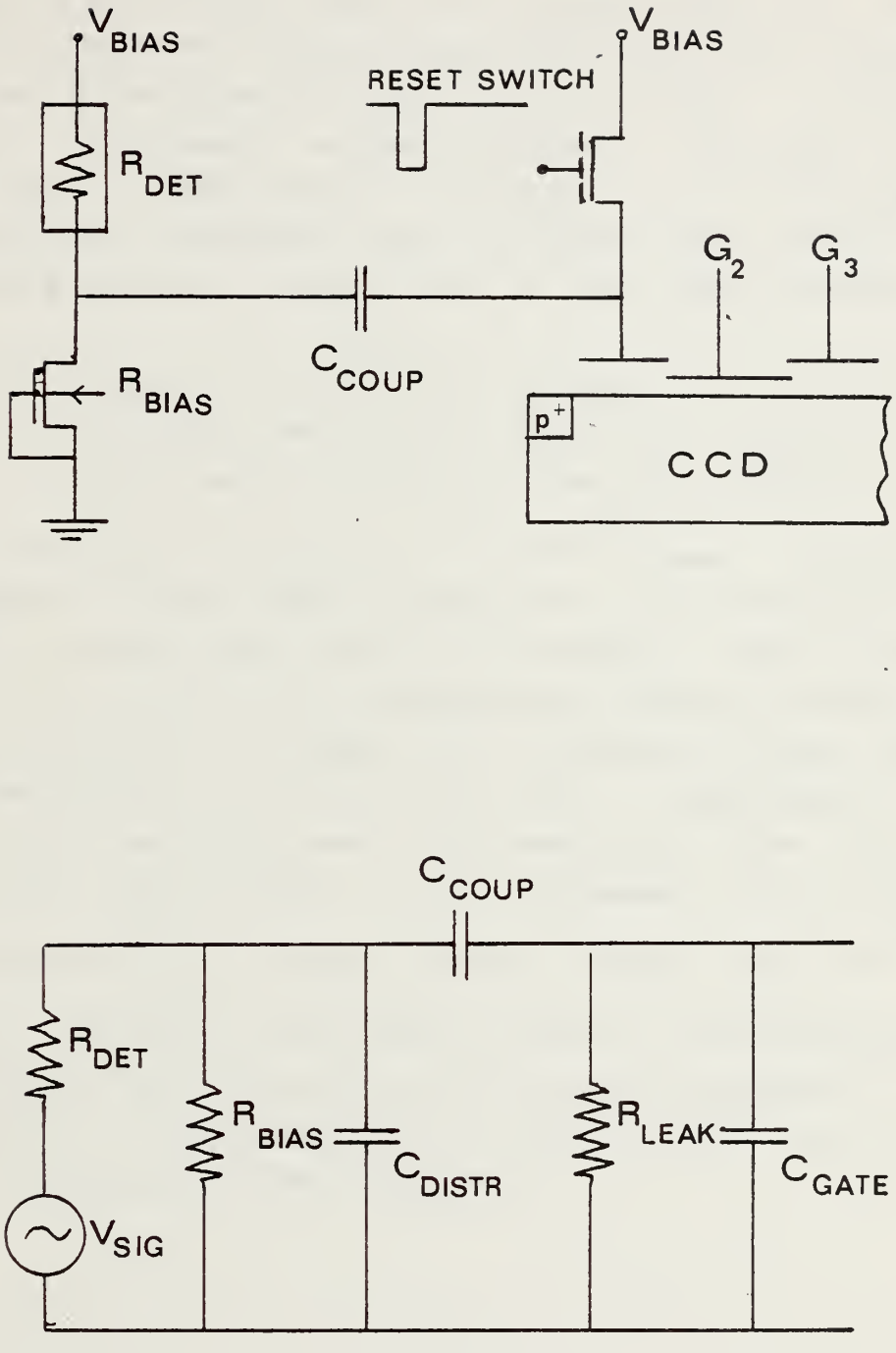


Figure 1 - INTERFACE CIRCUIT DIAGRAM

Thus, background suppression is achieved by isolating the dc-signal level from its ac-component. It will also increase, at the same time, the dynamic range of the CCD. In addition, the coupling capacitance will also isolate the dc bias of the detector and the CCD input. Furthermore, element to element nonuniformities, inherently connected with any IC fabrication process, are minimized by ac-coupling technique, thus minimizing fixed pattern noise, a serious problem in monolithic IR focal plane imagers.

The dc-bias of the gate capacitor at the CCD input is kept at a constant level, while the current flowing into the gate is quite small, limited by the gate leakage resistor, which has values of about 10^{11} to 10^{12} ohms. To prevent the ac-signal voltage being grounded via the gate power supply, a MOST is placed into the gate bias path. This transistor acts as a switch and periodically resets the bias level. When its channel is turned off, the detector sees only the RC combination of the CCD input gate. Experimental results with such a periodic reset structure have shown [3], that the bias level needs to be refreshed only every few milliseconds for a leakage resistor larger than 10^{11} ohm, without distorting the signal riding on this dc-level. The interface circuit arising from previous discussion is shown in Fig 1. Its equivalent ac-model is used for a computer aided frequency and gain analysis.

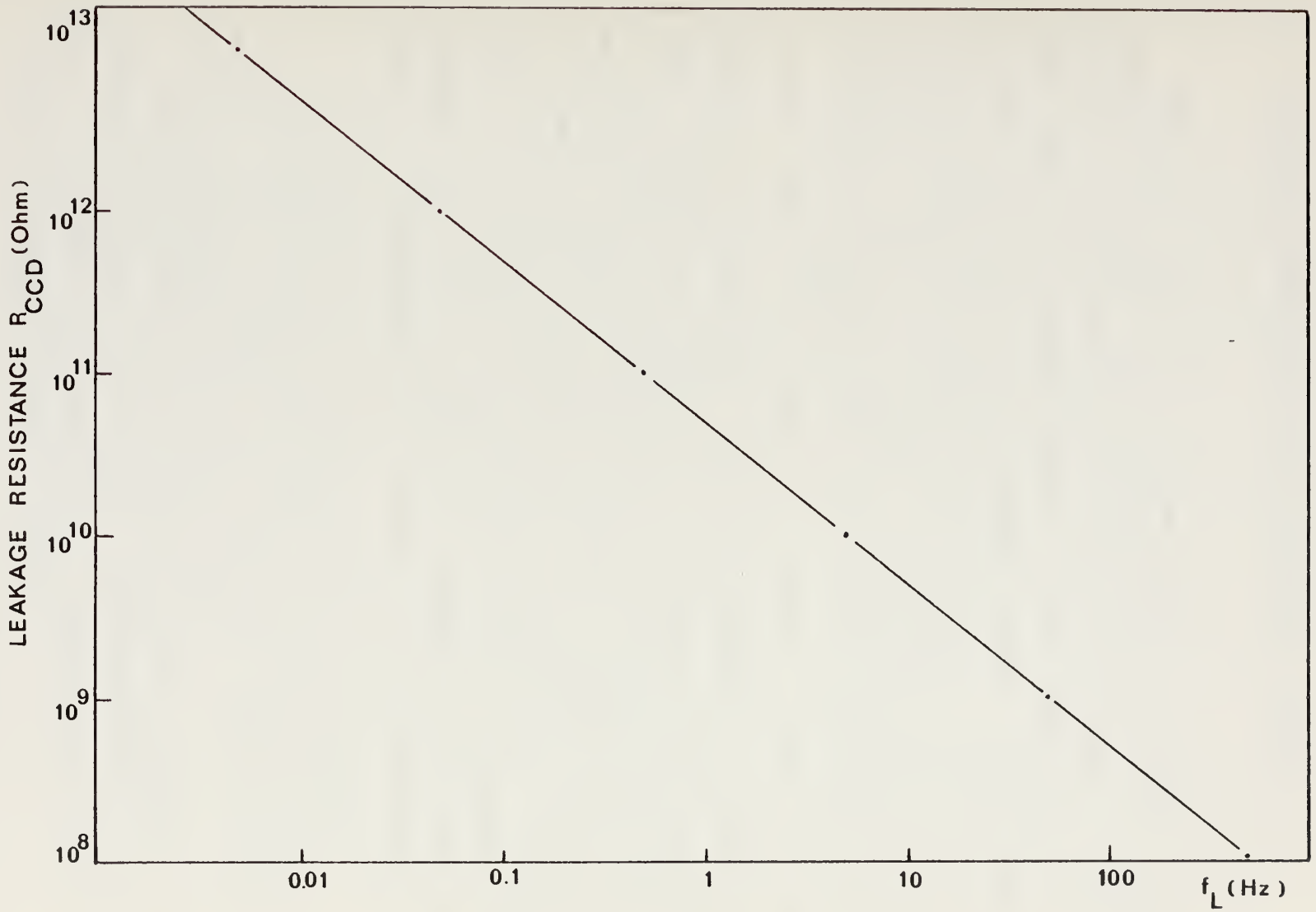


Figure 2 - CUT-IN FREQUENCY VS LEAKAGE RESISTOR

D. FREQUENCY ANALYSIS OF THE INTERFACE CIRCUIT

With the aid of a linear system analysis (LISA) computer program, the transfer function and the frequency response of the interface circuit is calculated. From the Bode plots for several values of the leakage resistance it is found, that the cut-in frequency corner (3db point) is mainly determined by this resistor value. Fig 2 shows the linear dependence of this cut-in frequency on the leakage resistor. Thus, to assure low frequency response without intolerable insertion loss, the leakage resistance must be larger than 10^{11} ohm, which is usually achieved with todays fabrication technology. The high frequency roll-off point (3db) depends on the ratio of detector to bias resistance. In two series of computer runs with LISA the Bode plots for reasonable values of bias resistors, ranging from 0.5 up to 10 megaohm, are calculated where the detector resistance is kept at 5 megaohm and 10 megaohm respectively. The results are shown in Fig 3. The variation of the insertion loss, midband gain Ao in db, is plotted on the same figure, showing its dependence on detector and bias resistance.

To summarize the conclusion from this analysis:

1. The leakage resistance should be as large as possible to achieve the desired low frequency characteristic and maintain sufficient high signal level.
2. The bias resistance, as the only design parameter, can be chosen to bandlimit the transfer characteristic to 10 to 20 KHz or to widen the bandwidth, if required, but only at the expense of a higher insertion loss.

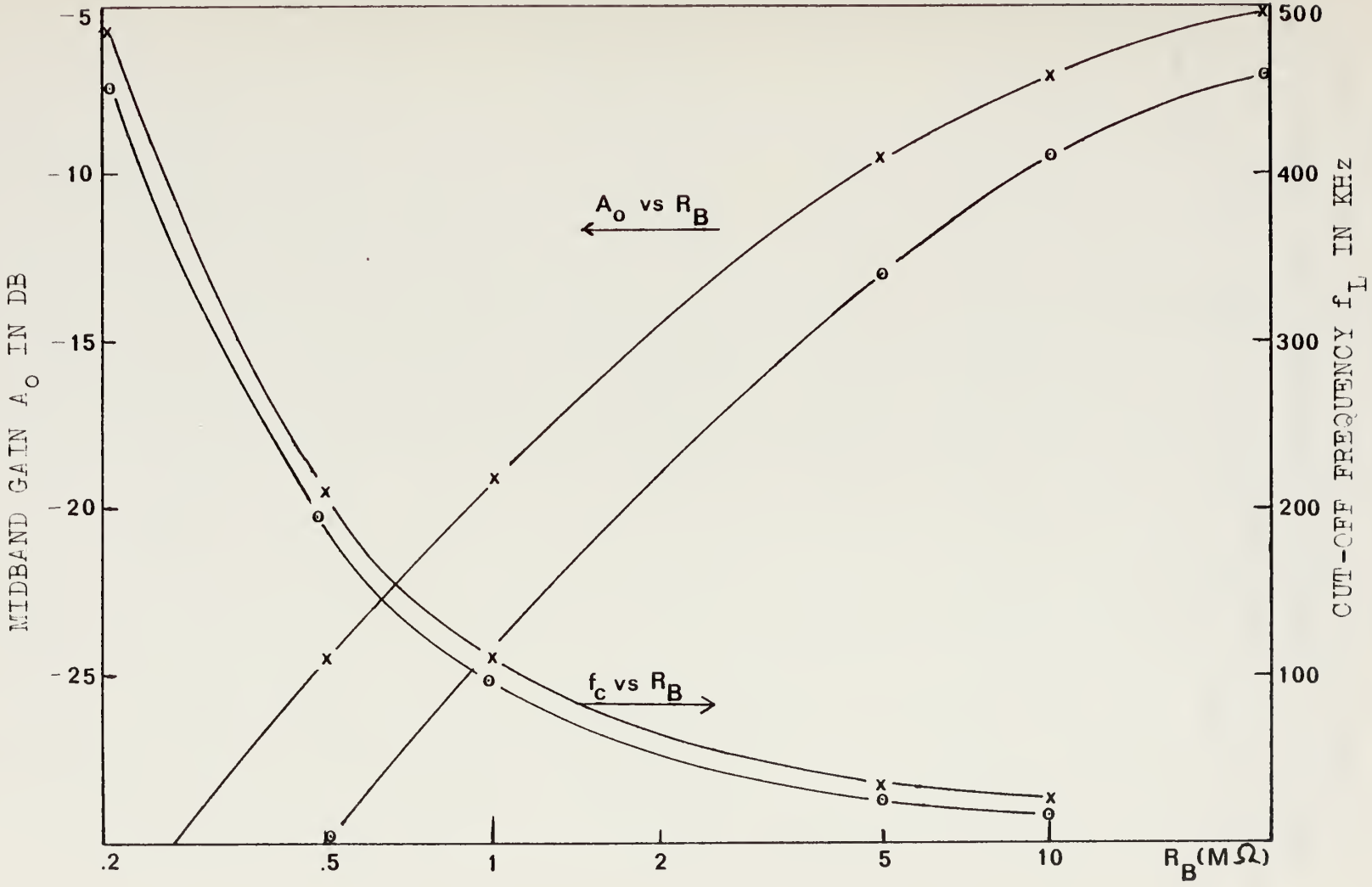


Figure 3 - GAIN AND CUT-IN FREQUENCY VS BIAS RESISTANCE

Using the minimum insertion loss of -7 db = 0.45, an overall gain from detector to CCD output of 3.37 is calculated, where the CCD is operated at a signal voltage gain of 7. How this CCD-gain factor can be achieved from the operating mode of the CCD will be explained in the next chapter.

III. CCD AMPLIFIER GAIN STUDY

It is not intended to give a qualitative analysis of CCD gain. But the fact, that a CCD shift register can supply a small to moderate signal gain is used in this study. Thus a quantitative explanation for different gain modes of operation is helpful to understand the noise problem associated with the electrical input of a CCD.

A. DESCRIPTION OF EXPERIMENTAL DEVICE

The device used in this study is a two phase, overlapping gate, P surface channel CCD, fabricated on n-type silicon substrate with <111> orientation. It was fabricated by TRW. A cross-sectional view is shown in Fig 4.

1. Input Stage

The input stage consists of an input diode which, when pulsed into a forward bias condition, acts as a charge supply. Four input gates, G-1 through G-4, provide several possibilities to store the injected charges in potential wells under the gate electrodes. G-2 and G-4 are polysilicon gates over a thermally grown silicon dioxide layer approximately 1000 Angstrom thick. A second layer of silicon dioxide was grown to a thickness of 3000 Angstrom, under the aluminum gates,G-1 and G-3.

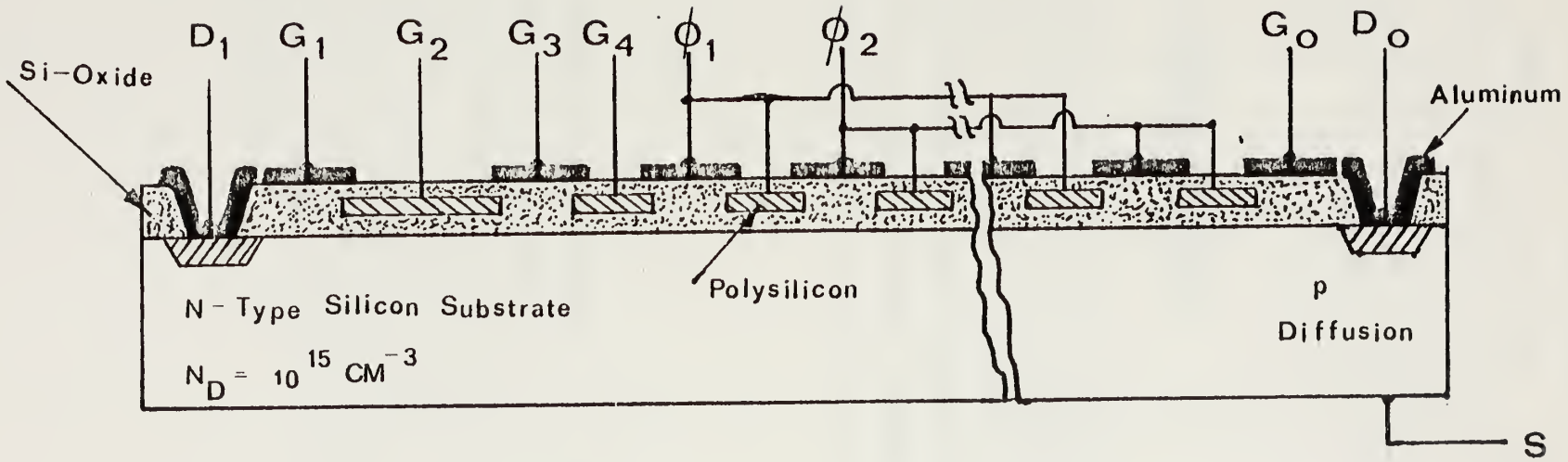


Figure 4 - CROSS-SECTIONAL VIEW OF 8-STAGE SHIFT REGISTER

All input gates are 1 mil wide and 0.8 mil long except G-2, which has a length of 3.2 mils. A signal voltage can be ac-coupled to any of these four input gates resulting in a signal charge packet under one, two, or three electrodes. The surface potential diagrams will help to explain the relation between the storage and the transfer in the channel.

2. Charge Transfer Channel

The channel consists of 8 pairs of transfer gates. A complementary symmetric clock waveform, -10 to -22 Volts, is used as phase 1 and phase 2 to each pair of aluminum and polysilicon electrodes. The surface potential beneath the stepped oxide allows only charge transfer toward the output stage. The channel gates are each 0.8 mils long and 1 mil wide.

3. Output Stage

The charge packet coming out of the transfer channel is sensed by the output diode,D-O. The output gate, G-C, is used to set a suitable surface potential in the vicinity of the output diode, to reduce fringing effects arising from the clock pulse. Two on-chip MOSFETs were used, one acts as the refresh MOSFET for the sensing diode. The second is the output driver operating in a source-follower mode with an external load resistor.

B. CCD TRANSFER CHARACTERISTIC

A signal voltage applied to one of the input gate is converted into a charge packet. This package is then clocked by the transfer channel gates to the output stage, where it is sensed, and an output voltage is developed across the external load. The static transfer characteristic, which plots the output voltage versus the input voltage, is obtained as followes: a slowly varying dc voltage is applied to one of the input gates. With the remaining input gates biased at selected dc bias conditions the dc output voltage after sample and hold circuit is plotted by an x-y recorder. The operating conditions are described as follows:

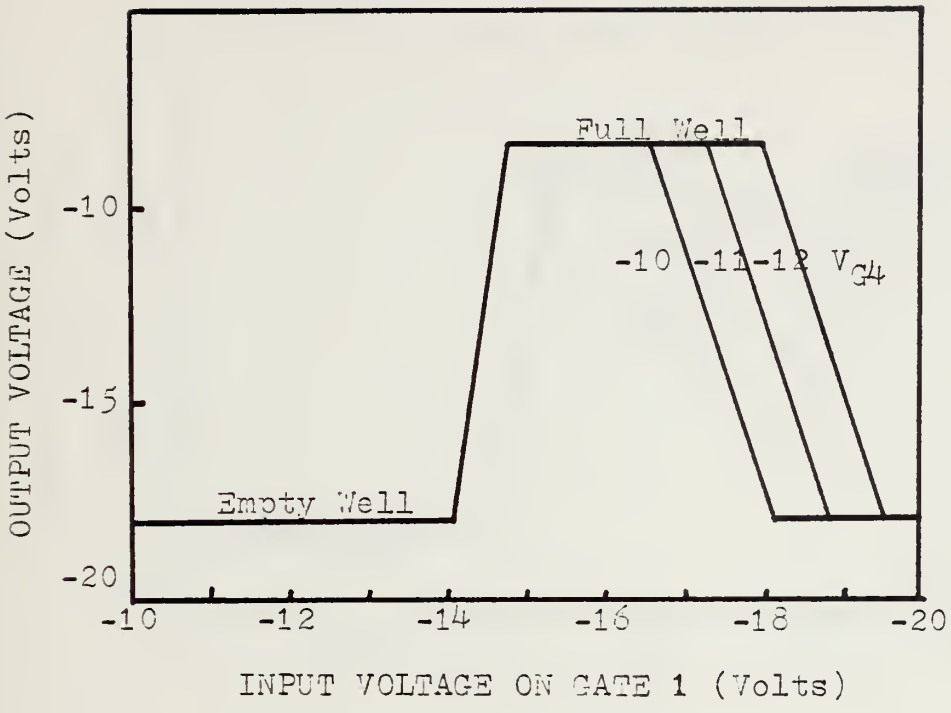
* Four clock pulses:

  input diode pulse from -2.5 to-12 V,
  reset MOSFET gate pulse from -18 to -35 V,
  CCD clock pulses from -10 to -22 V.

* Four dc gate biases:

  two unused gates at -26 V,
  output gate at -29 V and output drain at -35 V,
  external load= 50 Kohms,
  clock frequency= 20 KHz.

A typical set of transfer curves is shown in Fig 5 and in Fig 6.



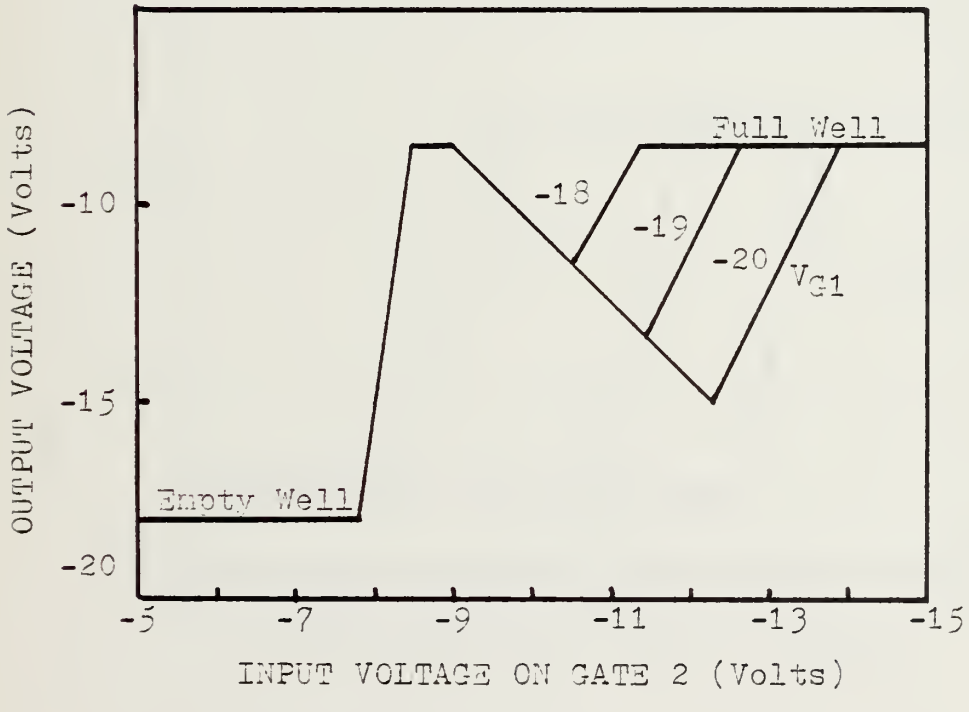
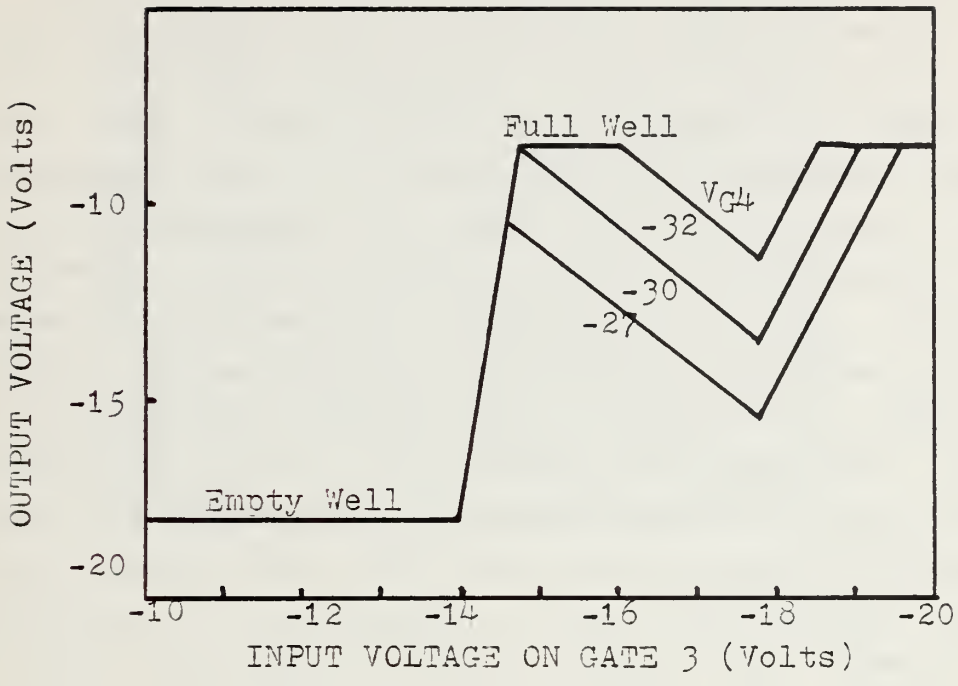


Figure 5 - CCD TRANSFER CHARACTERISTIC



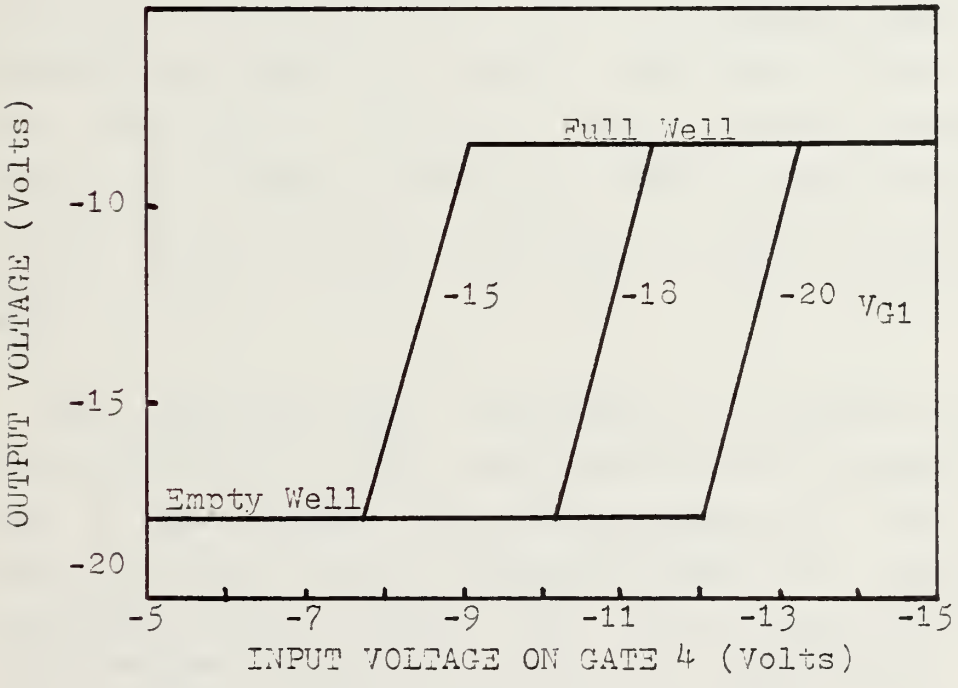


Figure 6 - CCD TRANSFER CHARACTERISTIC

The transfer characteristics are confined between two output voltage levels, corresponding to the empty well and the full well conditions. From these figures, it can be seen, that there exist three operating modes. Their mechanisms can be understood by examining the surface potential diagrams. The first is a high gain mode with inverting characteristic. The bias voltage on the input gates for this mode is approximately -7 V or -14 V. These values are determined by the threshold surface potential of the barrier gate, which can be either an aluminum or a polysilicon gate. This mode is quite nonlinear. The second mode is noninverting and characterized by a much lower gain but extends over a much wider bias range on the input gate. This mode can be achieved, if the signal charge package is stored in one, two, or three storage wells after a potential barrier which sets the "spill" limit after all wells have been filled. The height of this barrier is signal charge related. Therefore, neither the nonscuppering nor the noninverting mode is present, when gate 4 serves as input gate. The third or inverting mode appears, whenever the amount of charge allowed to enter the transfer gate is limited by a potential barrier in front of the signal storage wells. Thus, the input on gate 1 eliminates this mode.

The experimentally determined dc transfer curves show linear sections for the inverting and the noninverting modes over a bias range from one to five volts. The linearity shown in the static characteristics is confirmed by observing the ac input and output signal waveform on an oscilloscope. There is no noticable distortion, when the input peak to peak voltage stays within the linear range. Thus the CCD may be used as a linear small gain amplifier.

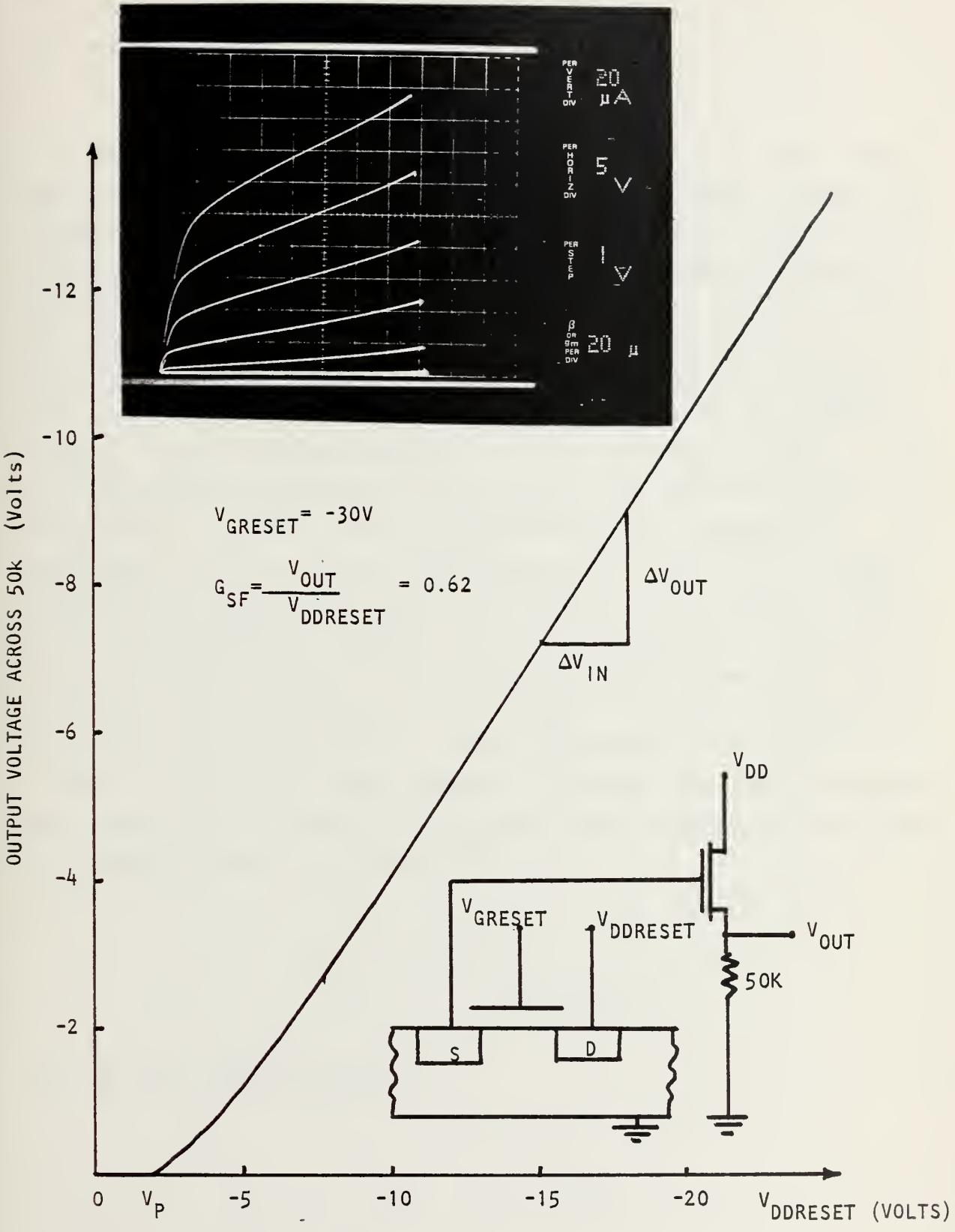


Fig. 7 OUTPUT MOSFET CHARACTERISTICS

C. CCD-GAIN

The overall CCD gain is the product of the input sensitivity (no.of charges/volt), the loss factor or transfer efficiency and the output sensitivity (volt/no. of charges). The output amplifier gain is usually included in the output sensitivity. The gain of the output source follower is determined from the transfer curve shown in Fig 7. The same figure includes the transfer characteristic of the output MOSFET from which a g_m = 39 micromhos is found. The responsitivity for the output stage was experimentally evaluated. A value of 0.8 microvolts/hole is calculated. From the responsitivity measurement an effective output node capacitance of 0.2 pF is found. Knowing the number of holes arriving at the output diode, the corresponding voltage can be calculated. During this study the exact number of charges created at the input stage has not been measured. Therefore, the input sensitivity could not be determined. Another approach to calculate the overall gain is used, instead. Knowing the input voltage and the effective capacitance, the signal charge package can be approximately calculated from:

$$V_{IN} = Q_s / C_{IN\ effective},$$

and for the output stage

$$V_{out} = Q_s / C_{out}.$$

Assuming that the transfer efficiency is approximately one, the CCD gain can be calculated approximately from:

$$G_{CCD} = C_{IN\ effective}/C_{out}.$$

From this equation the different gain factors are calculated for several possible input bias conditions. The capacitances are calculated from the gate geometry supplied by TRW: C1=0.052 pF, C2=0.71 pF, C3=0.05 pF, and C4=0.237 pF. The results are tabulated in matrix form. The experimental results from the static transfer characteristics are also presented in a similar table. Some agreements in the following trends are noted: (1) The occurance of inverting and noninverting modes are correctly predicted except that two noninverting modes have not been experimentally measured. The reason that two predicted noninverting modes could not be observed is the actual limitation of the transfer clock level at -22 V. (2) The gain factors agree within approximately 20%. The discrepancies are larger when the outside gates G1 and G4 are involved.

It is clear that a more refined physical model taking into acccunt the effect of the neighboring gate biases on the surface potential, the effect of different oxide thickness etc. is needed. But as a first approximation, the simple surface potential calculation based mainly on the gate geometry, serves as a helpful model.

CCD GAIN MATRIX

MEASURED GAIN

Constant Gate Voltage

Varying Gate Voltage	G_1	G_2	G_3	G_4
G_1		4.95	4.95	4.95
G_2	(4.95) 1.4		(4.95) 1.4	(4.95) 1.4
G_3	(4.95) 1.2	(4.95) 1.2		(4.96) 1.2
G_4	(4.95)	(1.4)	(1.2)	

CALCULATED GAIN

Constant Gate Voltage

Varying Gate Voltage	G_1	G_2	G_3	G_4
G_1		5.7	6.1	6.0
G_2	(4.6) 2.1		(4.4) 2.14	2.06
G_3	(4.5) 1.4	1.43		(4.3) 2.06
G_4	(7.3)	(2.1)	(1.8)	

(#) inverting mode

D. CONCLUSIONS

CCD as an amplifier has been studied. There are three operating modes possible, depending on the gate bias conditions, but only two modes provide adequate linearity for analog applications:

1. An inverting mode
2. A noninverting mode.

A simple analysis using the surface potential calculation establishes the operating conditions for both modes. The magnitude of the gain factor is a design parameter and depends largely on the geometry of the input gates.

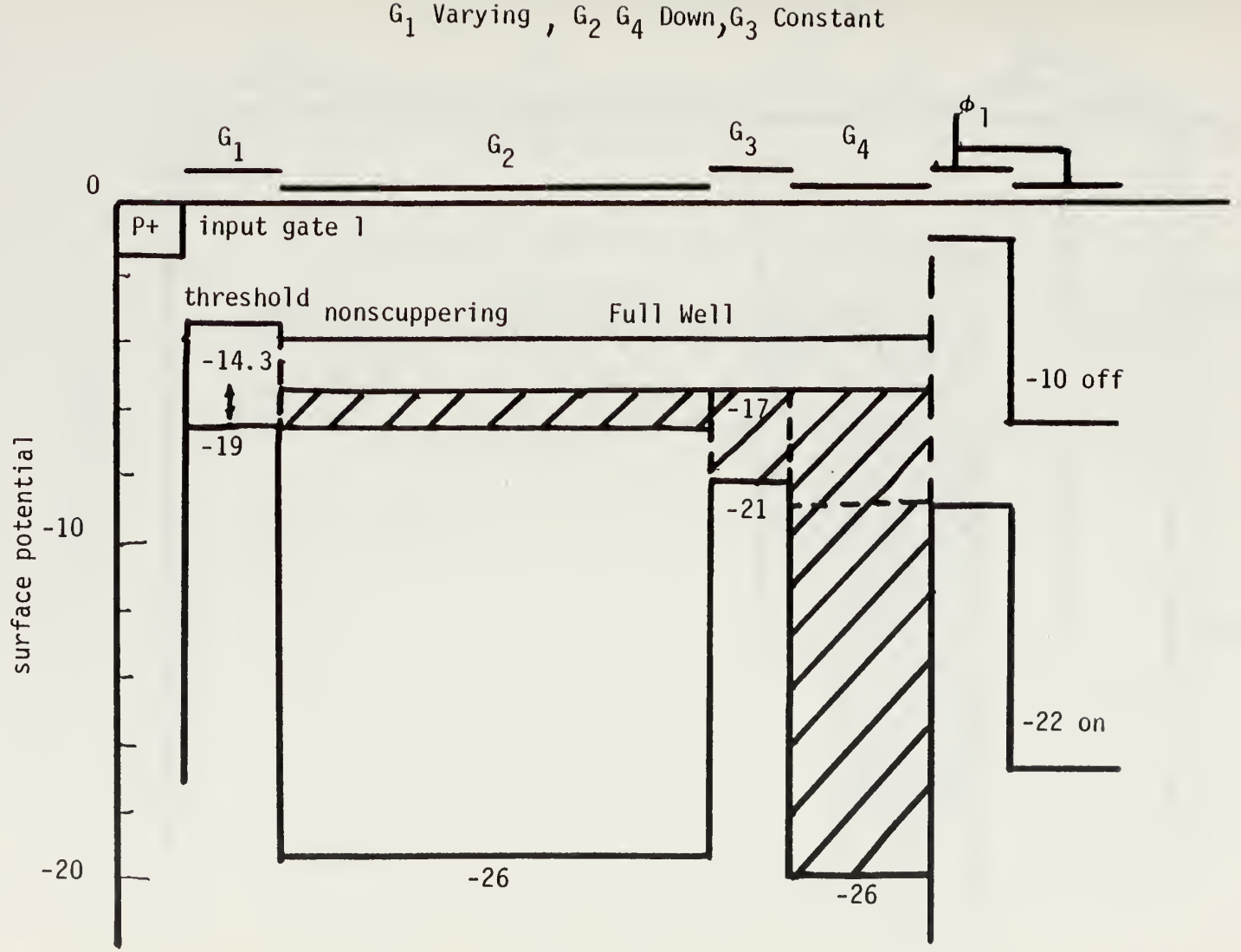


Figure 8 - SURFACE POTENTIAL DIAGRAM 1

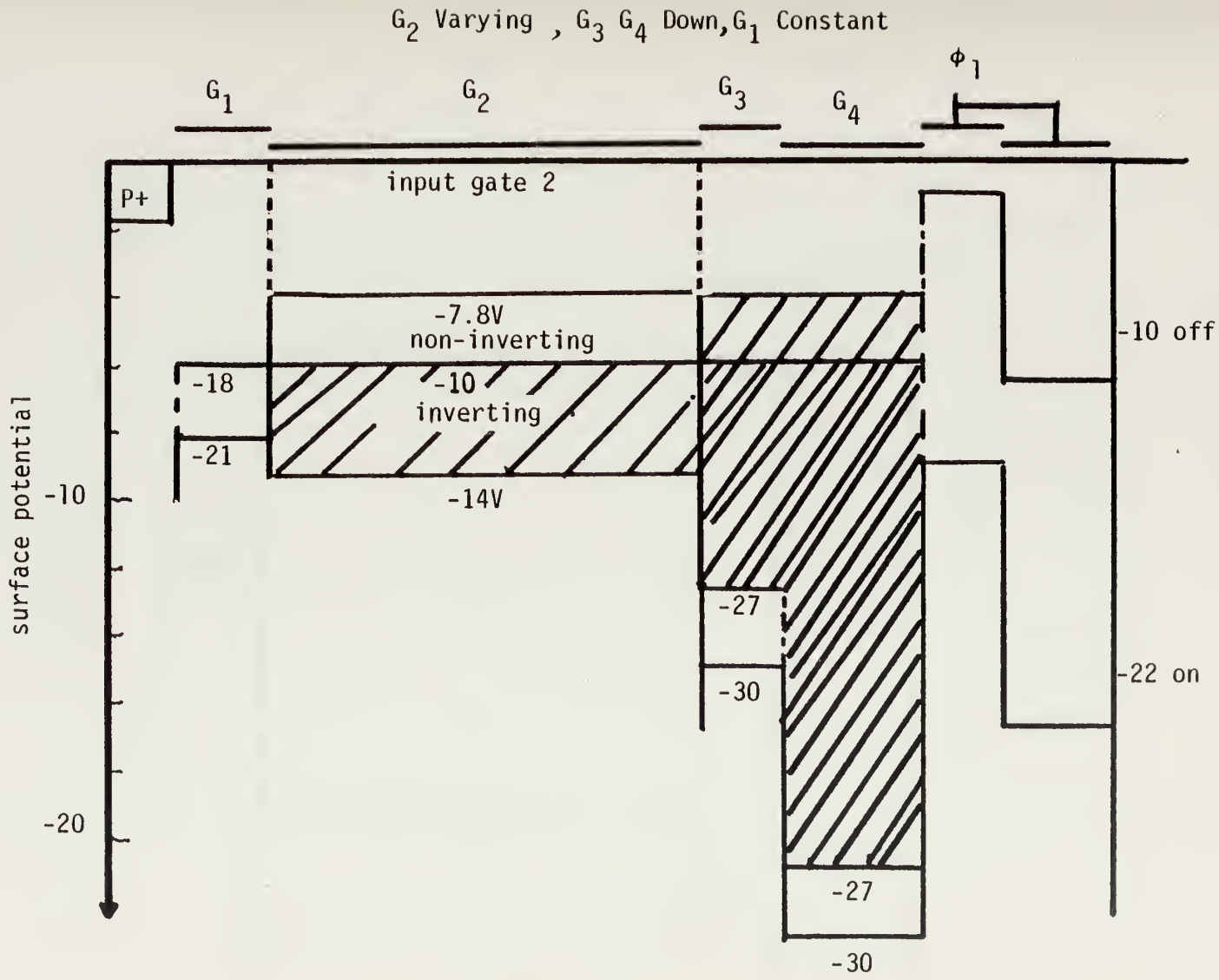


Figure 9 - SURFACE POTENTIAL DIAGRAM 2

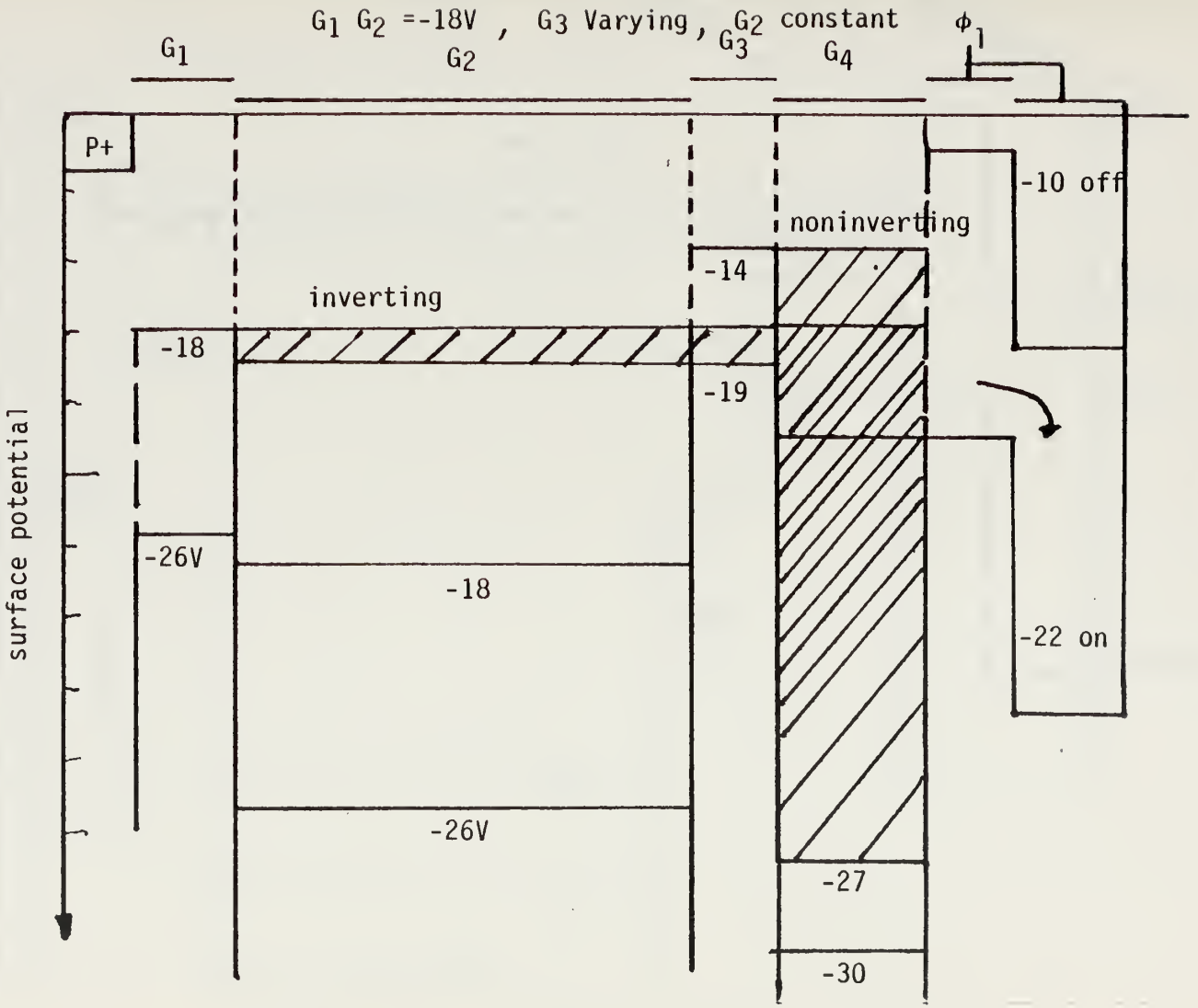


Figure 10 - SURFACE POTENTIAL DIAGRAM 3

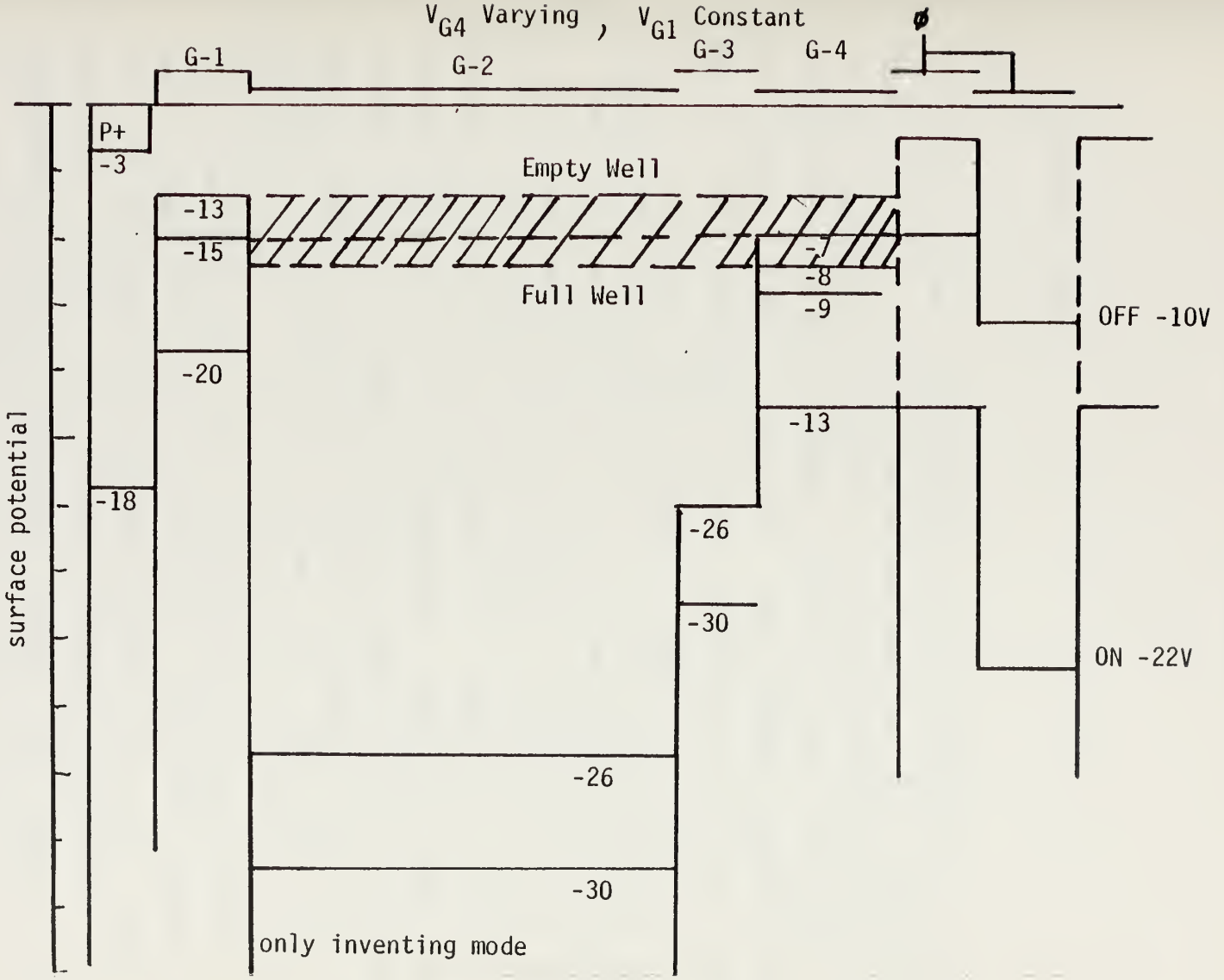


Figure 11 - SURFACE POTENTIAL DIAGRAM 4

IV. NOISE

A. DETECTOR NOISE

Three noise contributions can be identified in PbS and PbSe detectors. 1/f noise is dominant at low frequencies. At intermediate frequencies, generation-recombination noise is dominant for PbSe sensors, while for PbS detectors the 1/f noise remains dominant. The spectral region in which the 1/f noise dominates can be estimated by $BW=1/4\tau$, where τ is the detector time constant. Typical values of the time constant for PbS range from 800 to 4000 microseconds, giving a BW of 250 to 1250 Hz. For PbSe detectors, time constants around 30 microseconds are typical, resulting in a BW of 30 to 50 KHz. Thus, in the frequency region of interest, the noise spectrum is 1/f dependent, as shown in Fig 12 for typical PbSe and PbS detectors. Based on these spectral noise voltages, a sensor limited operation for the hybrid IR imager under discussion can be achieved, if the CCD noise, referred to the detector output, is 20db less than the detector noise. That is, the S/N ratio will not decrease, since the individual noise contributions from detector and the CCD amplifier add in quadrature, while the thermal noise from the bias and the interface circuit is two orders of magnitude below the detector noise and, therefore, can be neglected in the low frequency region. The third spectrum due to the Johnson or thermal noise will dominate only at high frequencies. Total spectral noise voltages depend on the operating conditions, such as the bias, cooling, and on individual detector materials and geometry (sensor area).

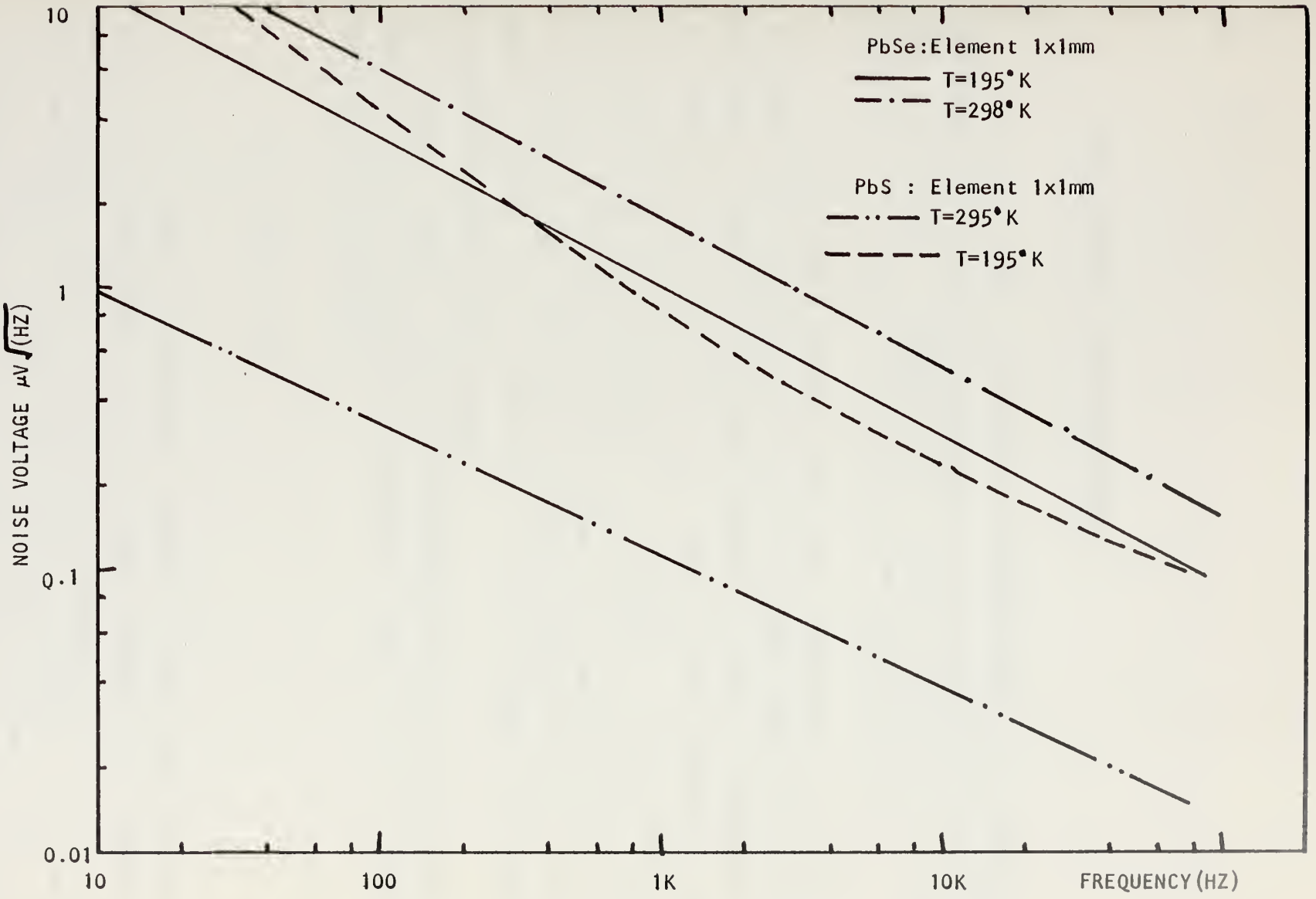


Fig.12 PbSe and PbS DETECTOR NOISE SPECTRUM

B. CCD NOISE

1. Theoretical Considerations

In a CCD -as shown in chapter III- the signal is represented by minority carriers in the inversion layer of a MOS structure. Consequently, noise in CCDs is often expressed in terms of noise equivalent electrons.[10]

Three noise sources have been identified in a CCD:
1. Input noise, arising at the input stage, where the signal voltage is converted to signal charges in the CCD channel.
2. Transfer noise, affecting the signal charge packet during its transfer along the shift register. Two origins of transfer noise are identified, the leackage current noise, that is continuously being added to a charge packet as it travels down the device and the fast-interface-state noise, which results in a variance of the amount of charge transferred each clock period.
3. Output noise, which is introduced after all transfers, when electronic charges are converted back to a discrete analog signal voltage.

a. Input Noise

This fluctuation exists in each charge package which is introduced by the input voltage or current. Analytically, input noise is the variance on the number of charges which the input capacitance is charged. Its mean square value depends on the input scheme used for introducing the signal; for example, input through a diode,

input thrcugh a gate , or the fill and spill method [9].

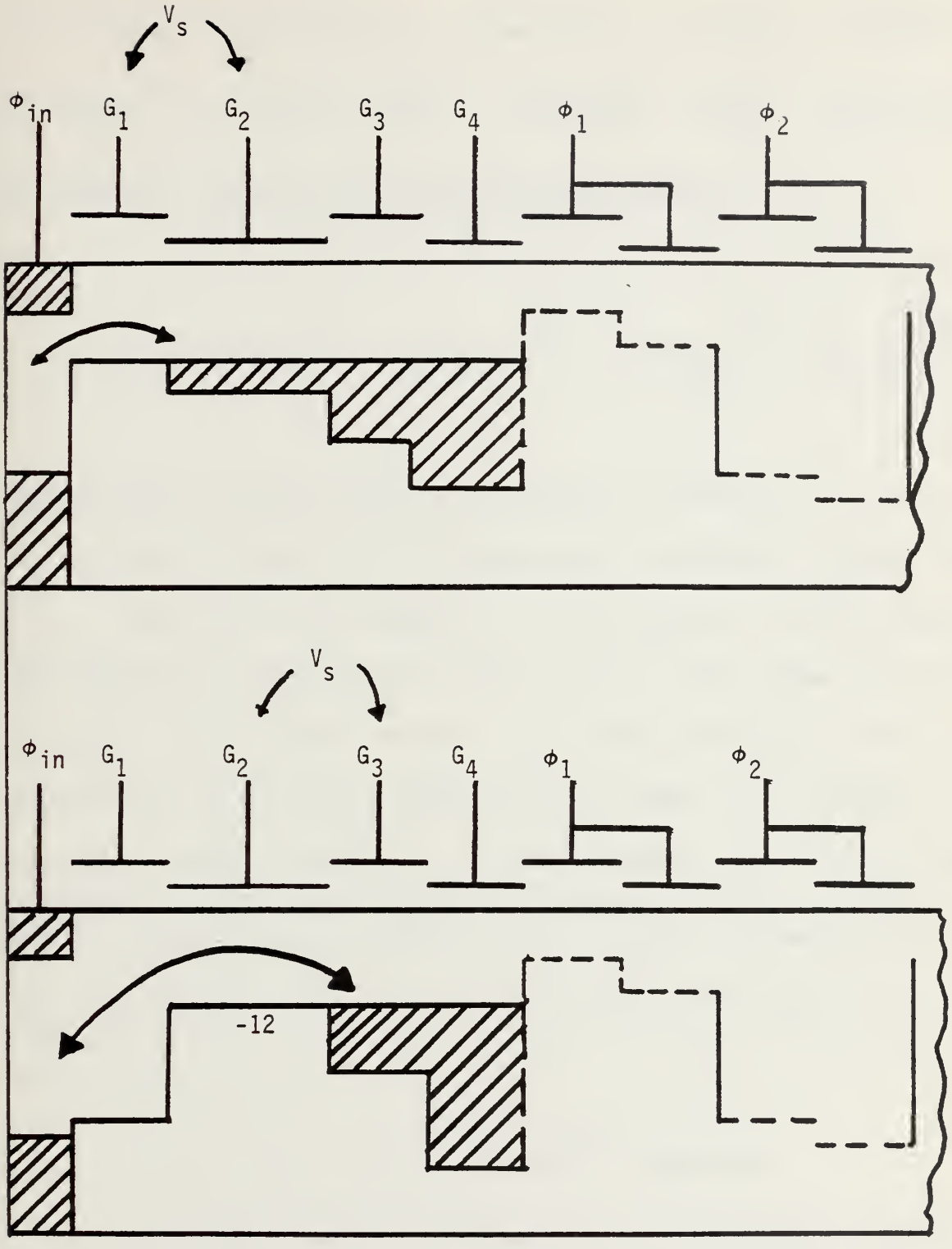
The ncise for the fill and spill input technique will be dicussed. The noise is independent of the signal amplitude, but is related to the input capacitor reset noise given by $(kT/C)^{1/2}$. A closer look at the input mechanism, shcwn in Fig 13, identifies this noise with thermal ncise in a MCSFET channel, under the holding well capacitor electrode G2 cr G3, draining excess charge frcm the virtual source inversicn layer. The region abcve the barrier of gate G1 cr G2 acts as a MOSFET channel,while the reverse biased input diode is collecting all charges crossing this barrier. A rigcrcus derivation cf thermal ncise in a MCSFET channel is given by [8], where the mean square fluctuation in the charge ccntained on the virtual source capacitor will becccme:

$$N_{IN}^{2} = 2/3kTC_{Source}.$$

In the lcw current regime, that is, the final stage, where the "spill" prccess becomes emissicn limited, this expressicn reduces to

$$N_{IN}^{2} = 1/2kTC_{Source}.$$

Since the scurce capacitor is reset through an effective MCSFET resistcr with a transconductance, g_m,



signal input on G_2 or G_3

Figure 13 - POTENTIAL EQUILIERATION METHCD FOR CCD INPUT

an internal band-limiting mechanism is given by NEBW = $g_m(2\pi C_s)^{-1}$. Using this effective noise equivalent bandwidth, the average noise voltage becomes:

$$V_n = (1/2\ kTC_s)^{1/2} / (g_m/2\pi C_s)^{1/2} = (\pi kT/g_m)^{1/2},\ V[Hz]^{-1/2}.$$

In the low current regime g_m becomes very small, $g_m = qI/nkT$, where n is an empirically measured factor of 1.4. Thus the g_m should be determined by the current flowing in the channel under the barrier gate, when the last fraction of excess charge is being removed from C_s. Referring to [6], the transfer of the last 0.1 percent of signal charge requiring about thirty normalized time constants without the aid of a fringing field. From the curves given in the reference, 0.1 percent corresponds to a voltage change of 10^{-2} volts, or in terms of charge for G1 (case 1),

$$\Delta q = C1\Delta V = 4.45 \times 10^{-16} \text{ coulombs.}$$

When the barrier channel is turned off relative to the virtual source, a quasi-static equilibrium is achieved, and the above charge, Δq, must diffuse through a channel length of 15 microns. The normalized time constant for gate one is:

$$t_r = I^2/\mu = (15x10^{-4})^2/100 = 22.5 \text{ nsec, so that}$$

$$I = \Delta q/30t_r = 4.45x10^{-16} / (30x22.5x10^{-9}) = 0.67 \text{ nA.}$$

Substituting these values in

$$g_m = qI/nkT = 1.85x10^{-8} \text{ mhc,}$$

giving an input noise of

$$V_n = (\pi kT/g_m)^{1/2} = 0.838x10^{-6} \text{ Volts/Root Hertz,}$$

and a noise equivalent bandwidth of

$$NEBW = g_m(2\pi C1)^{-1} = 66.16 \text{ KHz.}$$

Then the total noise power is:

$$P_n = V_n^2 xNEBW = 4.65x10^{-8} \text{ Watts} = kT/2C1.$$

For the second input bias condition (case 2), where the barrier gate is G2, with L= 3.2 mil, $t_r = 6.4 \times 10^{-7}$ sec, I = 0.37 nA, $g_m = 1.02 \times 10^{-8}$ mhos, the spectral noise voltage is calculated as:

$$V_n = 1.128 \times 10^{-6} \text{ Volts /root Hertz,}$$

where the NEEW = 2.286 KHz.
The total noise power becomes:

$$P_n = 2.9 \times 10^{-9} \text{ watts} = kT/2C2.$$

Because the CCD is inherently a sampling device, it is essential to bandlimit the noise and the signals below the Nyquist frequency to prevent aliasing. The interface circuit, discussed earlier, assures the bandlimiting of signal and noise before they enter the CCD. But there is no bandlimiting mechanism for the noise generated internally within the input circuit. Thus it is important to know, how fast the device must be clocked to prevent aliasing of noise.

The results calculated above are applied to the concept of aliasing or foldover in a sample and hold action as outlined in appendix B. A plot of spectral noise density vs sampling frequency is given in Fig 14. Clearly, this demonstrates which input mode should be used to minimize (1) the overall input noise for $f_s \geq 2BW$ and (2), if a lower

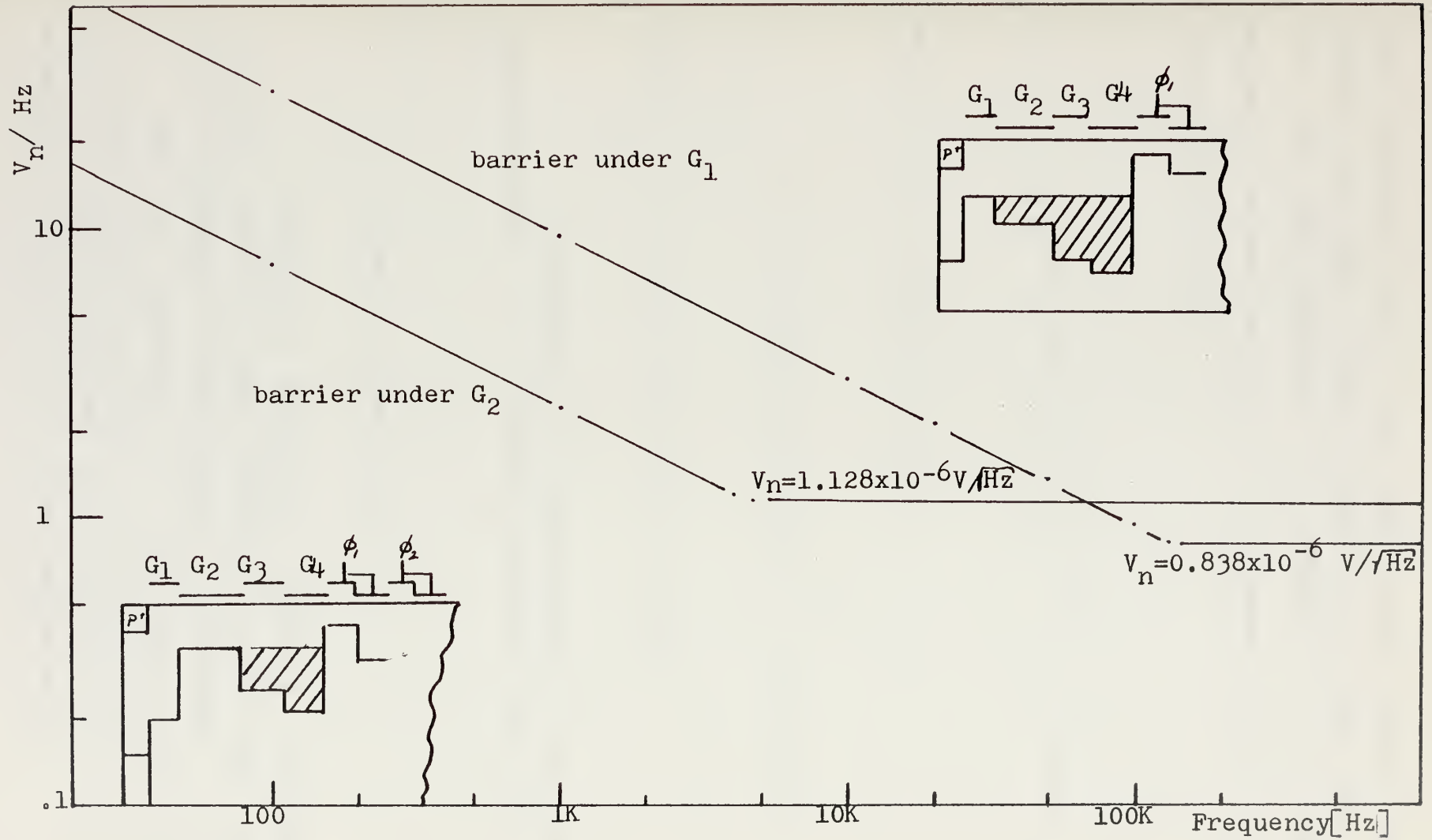


Figure 14 - SPECTRAL NOISE DENSITY VS SAMPLING FREQUENCY

clock frequency must be used, what is the tradeoff between a higher noise level without aliasing and a lower noise level, but with some aliasing. As an example, at f_s = 20KHz, the equivalent noise electrons (for p-channel holes) for case 1 are calculated as:

$$n_e = C1V_n(\text{at } f_s/2) \times (f_s/2)^{1/2} / q = 61 \text{ holes},$$

and for case 2 without aliasing:

$$n_e = C2V_n(\text{at } f_s/2) \times (f_s/2)^{1/2} = 500 \text{ holes},$$

where V_n is read off from Fig 14 directly.

To bandlimit this input noise the anti-aliasing characteristics of the floating diffusion input can be used [10].

b. Leakage Current Noise

Thermally generated minority carriers are collected along the shift register in such a way, that they do not experience the same number of transfers. This type of noise is equivalent to the noise associated with optically generated carriers. It is characterized by shot noise and can be expressed by the variance of the number of electrons introduced into a given charge packet:

$$N^2_{Leak} = 1/q\ Q_{Leak}\ ,\ [electrons^2]\ .$$

If the dark current is given by a leakage current density, J_L [amps/cm^2], then the expected value of the random variable Q_L is,

$$Q_L = A_{eff}\ J_L\ \tau\ ,\ [coulombs]\ ,$$

where A_{eff} is the current collecting area and τ is the corresponding integration time , which is given by the reciprocal of the clock frequency.

c. Fast Interface State Noise

In surface channel devices, fast-interface-state noise results from fluctuations in the number of charge carriers emitted from the fast interface states during each transfer[8]. Each time, a charge packet is transferred under a CCD electrode, it fills the surface states in the semiconductor-insulator interface. At the following transfer some of these charges are reemitted into the charge packet. For the following charge packet, some charges add or subtract from it, thus it is dependent on the charge subtracted or added to the previous packet. Carnes has shown that this variance is given by:

$$N_s^2 = pAkTn_s \ln(2) \ , \ [\text{electrons}^2] \ ,$$

where A is the gate area, k is the Boltzmann's constant, T is the absolute temperature, ns is the surface state density, and p is the number of phases. For a two phase shift register the quantity of noise electrons, n_f , introduced into a given packet for each transfer, is:

$$n_f = [\ N_s^2\ ]^{1/2} = [\ 1.4\ kTn_sA\ ]^{1/2} .$$

It should be mentioned, that this type of noise is highly correlated with the previous and the following charge packets.

d. Output Noise

For the readout, using a floating diffusion or integrating diffusion, a capacitive node is preset to a reference voltage before the CCD charge packet is introduced. The uncertainty in the charge after preset represents the noise source. An expression similar to the input noise is given by [1]

$$N_{Res}^2 = kTC_o/q^2 \ , \ [\ \text{electrons}^2\ ] \ ,$$

or for $T = 300^{o} K$,

$$n_s = 400 \left[C_o (pF) \right]^{1/2} , [\text{ electrons }],$$

where C_o is the output node capacitance, which is the combination of the reset and the output diffusion and the gate capacitance of the output MOST amplifier.

A more detailed analysis for an " on chip" MOST is given in appendix A.

V. IDEAS OF SIGNAL PROCESSING ON IR FOCAL PLANE

A. INTRODUCTION

With the advance of CCD technology in IR imaging area sensors, more sophisticated signal processing schemes will become realizable. Besides simple readout and time-delay and integration (TDI) which already has been demonstrated for a linear array IR sensor, techniques and theoretical development similar to those worked out for day-light or low light TV compatible CCD area imagers, will influence the progress in signal processing on the IR focal plane.

Making use of the terminology of Information Theory, the focal plane is a source of information, where each picture element contains bits of information. The total amount of information provided by this source is fixed by the sensor physical limitations. The IR focal plane is clearly a source of low entropy, containing a lot of redundancies, since only the contrast -for IR devices defined as temperature differences- is of interest. Large portions of any image have the same intensity, thus contributing very little to our goal of detection or recognition. Only the spatial or temporal changes in signal strength can be used to discriminate against the so called background. Therefore, the basic idea of any processing is to maximize the source entropy, which must be done on the focal plane prior to further transmission. This process of changing the source entropy is called image or source coding in a wide sense. Source coding can be realized in spatial domain or

in some transform domain which will be dicussed in the following sections.

The entropy of a scene and its Fourier transform are identical; and this is true for any image transform whose Jacobian is unity [12]. This garantees that the process of maximizing the entropy will be independent of the domain in which we decide to work on.

The importance of this concept is apparent when visualizing that real-time signal processing is limited by its associated transmission channel capacity. Therefore, by increasing the source entropy, more vital information per unit time can be transmitted, or in other words, the time between imaging and recognition, or even identification is accomplished in real time. Clearly the total amount of information can never be increased as we go along the process line, but each bit of transmitted signal is weighted much heavier and is therefore of greater importance. This leads directly to error correcting signal coding, when transmission over a noisy channel must be used to assure that every transmitted signal is correctly received.

In the following sections possibilities of signal processing in spatial and transform domains are discussed.

B. PROCESSING IN SPATIAL DOMAIN

1. Introduction

As pointed out before, signal processing on IR focal plane can be done in spatial domain, where the independent variables are discrete values of the x,y coordinates of the

focal plane, while the dependent variable, the signal strength, is continous in range. Therefore, the signal is discrete analog or sampled analog in nature.

The solid state IR image sensors can be grouped into monolithic and hybrid structures. The distinguishing feature of monolithic devices is that both the sensor and the transfer section are built up on the same semiconducting substrate. All, but the Schottky barrier CCD, use the same metal-insulator-semiconductor (MIS) structure. The bandgap of these semiconductors (i.e. InAs, InSb, PbTe, PbSnTe) determines the absorption peak and, therefore, the useful IR region, they are operating in.

Charge injection devices (CID) use injection into the bulk for readout rather than the shifting transfer principle of the CCDs. Infrared applications of CIDs are reported by Kim[4] with InSb. Experimental work is currently undertaken to evaluate the MIS feasibility of narrow band semiconductors with large dielectric constants. (Tao, Belrose, 1976).

In hybrid devices, as discussed earlier, a SiCCD is used as a readout and preamplifier for an array of IR detectors, but can be extended to area sensors. In the following discussion the hybrid device is considered as the basic sensor structure.

2. Basic Processing Steps

Simple readout and preamplification is already presented in great detail in part II.

3. Time-Delay-Integration

If a particular point of a scene is mechanically scanned over a linear sensor array in the same direction as the charge transfer occurs, so that the contribution from each sensor element is subsequently added to the previous one, then this process is called time-delay integration(TDI). TDI results in a larger dynamic range, and a reduction in fixed pattern noise arising from sensor element nonuniformities . Furthermore, the S/N ratio is improved, too. The signal is added linearly, while noncoherent noise adds in a square root manner. Thus an improvement factor of the square root of the number of elements in the TDI can be achieved.

4. Advanced Signal Processing

Any process which involves some kind of decision rule, i.e. target present or not, target stationary or moving, will fall under this category. This advanced processing can be subdivided into

* Detection
* Recognition
* Identification.

A functional block diagram of a threshold detector and a moving target indicator (MTI) is shown in Fig 15. The threshold detector is made up by a sensor-clock generating circuit and a comparator. Its function is explained as follows: the area sensor is organized in a parallel-serial readout scheme, such that each element -row by row- is clocked out and send to a comparator.

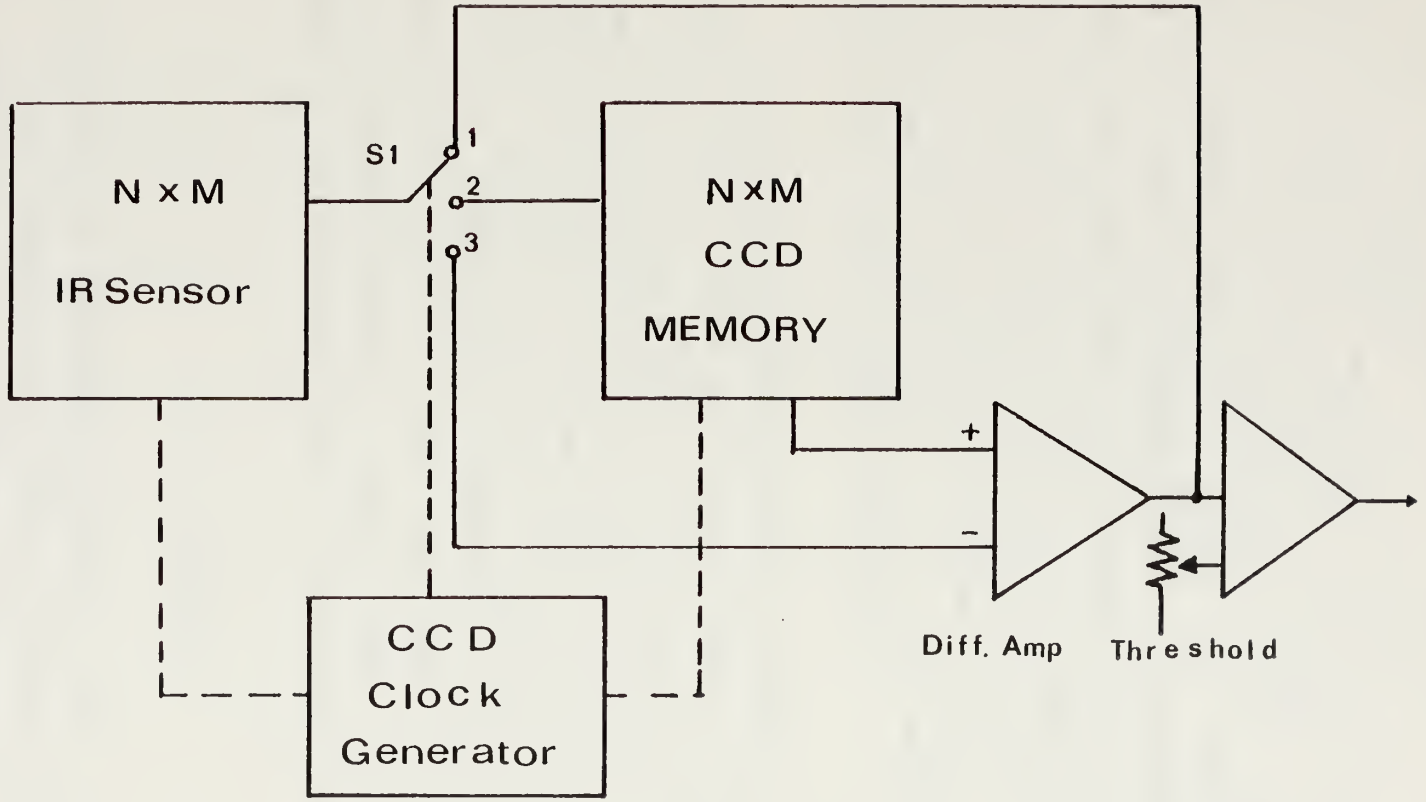


Figure 15 - THRESHOLD AND MOVING TARGET INDICATOR

If a preset threshold level is overcome, the output of the comparator can trigger some indicating device or may be used to switch from detection to MTI mode. In this mode the CCD-memory -identical in structure as the sensor parallel-serial shift register- stores one full frame and at the end of this storage cycle S1 switches to position 3. During the next cycle the present readout frame is compared with the stored frame on an element by element basis. A frame to frame subtraction is accomplished. Only those elements whose amplitude is different from frame to frame time will generate an output by the differential amplifier. Using a 100x100 interline transfer CCD imager (Fairchild CCD 201), an extension of this processor unit for TV display has been implemented and shown to be a very versatile device for low-light TV image signal processing.

A very simple technique for estimating the speed of a moving object from a television signal is described by [13]. This technique seems to be equally applicable to an IR image processing unit previously explained. This kind of process can already be categorized identification, if the evaluated target speed can be identified with some typical target speed signature. To describe the speed measure it is referred to Fig 16. From the frame to frame subtraction unit the frame difference signal (FDS) may be obtained. Summing up the absolute value of the differences, a quantity

$$S1 = \sum |FDS|$$

is obtained which increases linearly with speed. If the size of the imaged area would be the same for all targets, this would provide an adequate measure of speed. This constraint can be overcome when S1 is normalized by a measure of the size and detail of the moving image.

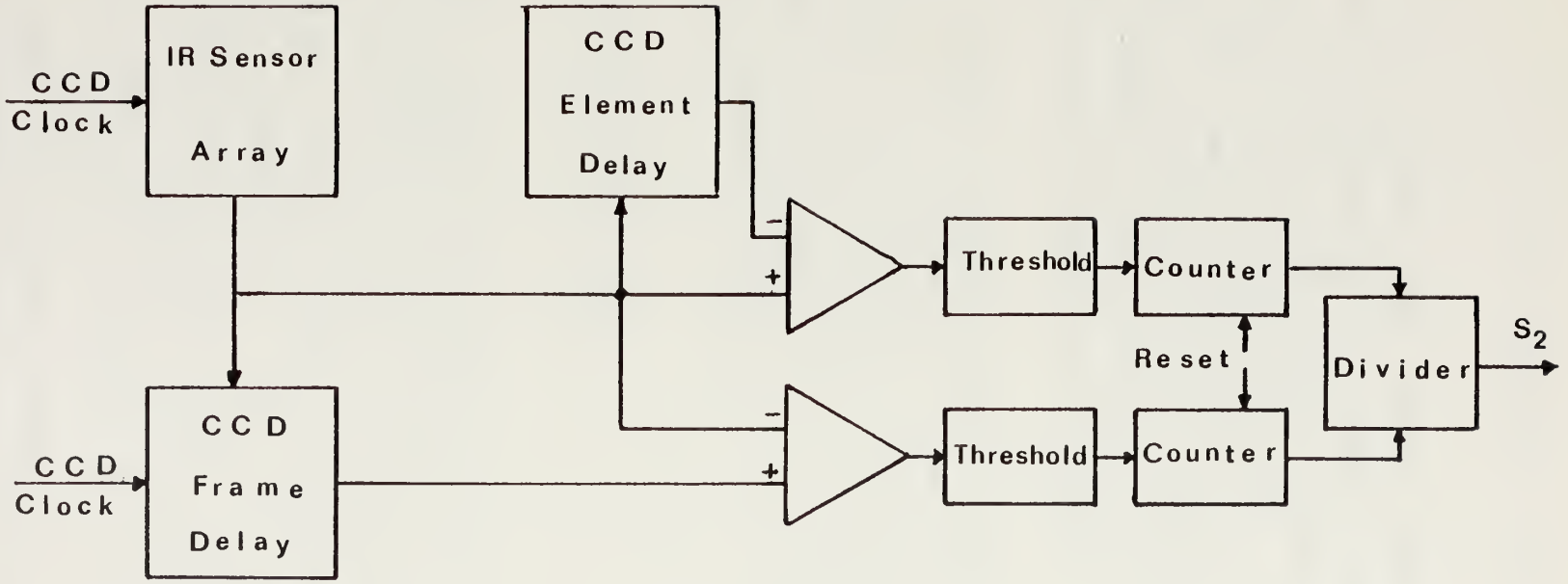


Figure 16 - BLOCK DIAGRAM OF A SPEED MEASUREMENT SYSTEM

That is:

$$S2 = \sum |FDS| \; / \; \sum |EDS|,$$

where EDS denotes the element difference signal. It is obtained by subtracting the value of the previous picture element from the value of the current picture element. The accumulation can be simplified when threshold devices are placed into each signal path and two binary counters represent the numerator and the denominator of S2. After a binary division of the contents in the two counters a fairly accurate speed estimate will be given.

Another sophisticated array processing can be achieved when a transversal filter is integrated into the focal plane; and filtering action takes place, while the information is read out from each element. This will be discussed in more detail in the next section. It is called the convolutional scanning [74].

C. CONVOLUTIONAL SCANNING

Today common scan technique in IR work is still to scan a single element in two directions, or to scan a line of elements in one direction, by mechanical means. Weight and complex post sensing signal processing usually prohibit real-time processing. But for numerous military and civilian applications, as in space surveillance, ballistic missile early warning, and tactical weapon systems, real-time processing capability is of vital importance.

So far, all signal processing is done off the sensing chip. The technique described here will explain how signal

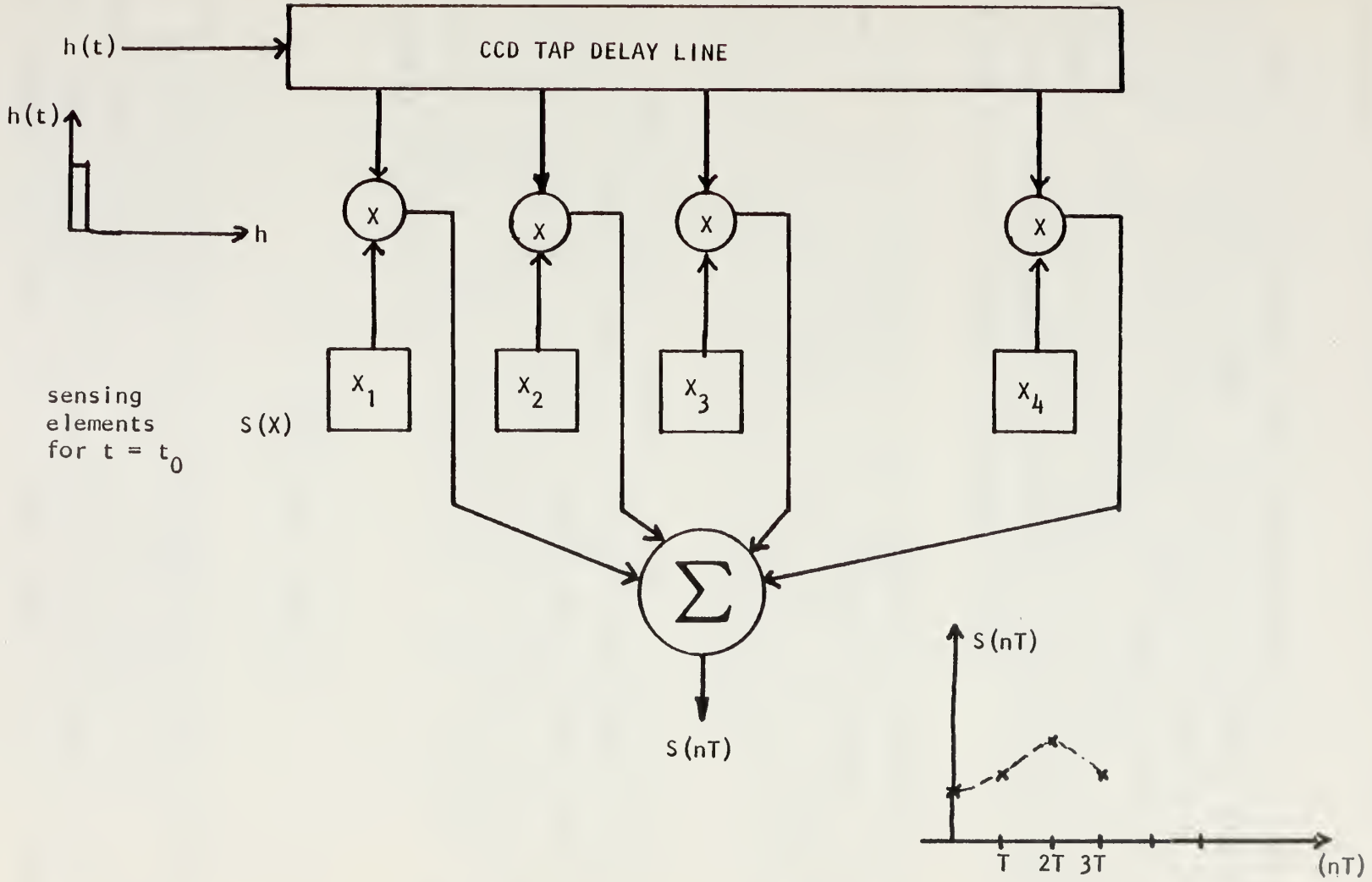


Figure 17 - CONVOLUTIONALLY SCANNED ARRAY

processing can be done directly within the detector array. Convolutionally scanned one or two dimensional IR arrays will have a profound impact on future focal plane signal processing.

The hybrid approach offers the advantage to combine IR detectors and CCD delay , or CCD tap delay lines to a convolving processing unit. The design of the taps of an integrated transversal filter determines whether a simple readout scheme , or a Fourier transform is being implemented. Thus by properly choosing the impulse function h(t) for the tap weights, the desired signal format will be available at the sensing processor output.

The basic structure of a one dimensional convolutionally scanned array consists of the following elements, see also Fig 17. Each array element output and its corresponding delay line tap are connected to a multiplier; the sum of the multiplier outputs is the scanned array output.

A convolutionally scanned array, as in Fig 17, is a linear transversal filter . A linear transversal filter is a delay line with equally spaced taps, whose outputs are weighted and summed to form the filter output. This output is the input signal convolved with a scaled version of a sampled analog signal weighted by the filter taps. Expressed in close form:

$$y_i(nT) = \sum_{i=0}^{N-1} x(nT)\ h(n-i)T.$$

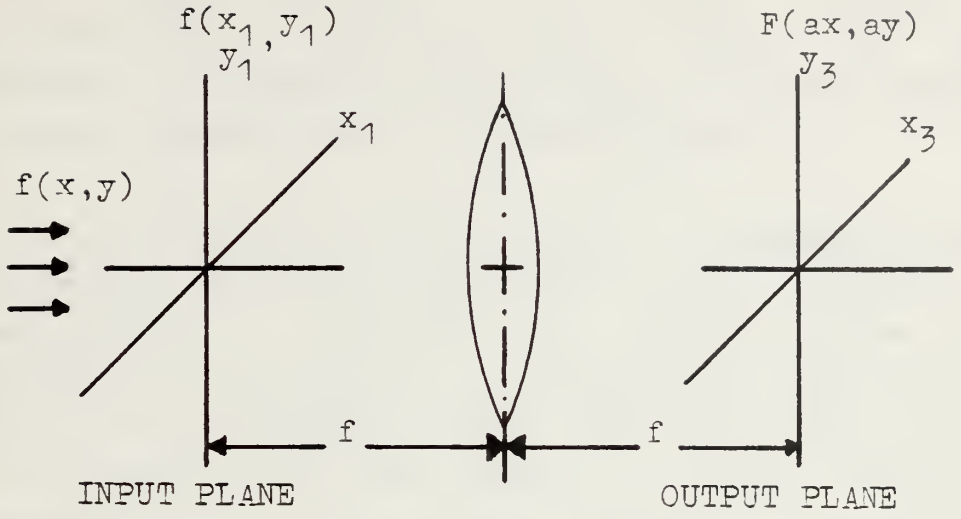
In the described array, the tap weights are continuously set by the instantaneous values of each sensor output. These values are time-varying, but spatially sampled data of the wave field incident on the array. If the transfer time of h(t) through the delay line is small relative to the period

of the highest frequency component in the incident wave, then the signal in the array elements is fixed in time and only a spatial convolution -not temporal- is carried out. The signal at the system output is formated into samples of a function at discrete time intervals. If this convolutional scanning is carried out repeatedly at a rate, such that the sampling criterion for the incident signal is satisfied, then the time varying information can be extracted from this convolutional scanning process. For typical IR targets of interest, their signatures are usually fairly slow temporally varying signals, such that even with slow scanning rate all the information would be preserved: important feature for special military applications in space surveillance.

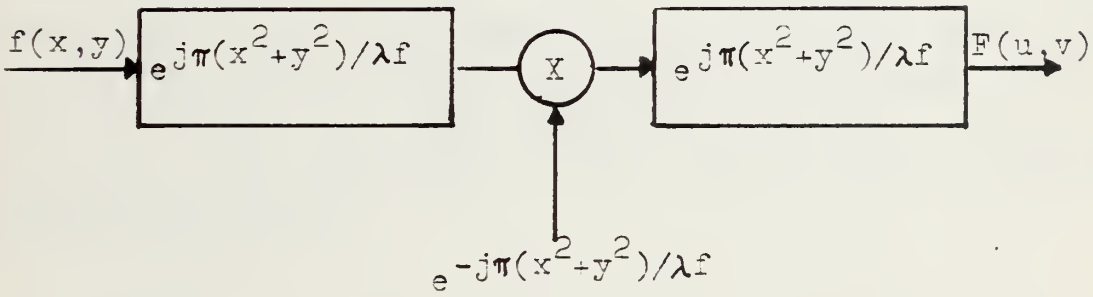
The scanning function has not been specified . It is a discrete sampled analog version of h(t) for the CCD tapped delay line. As a first example, an impulse function is chosen as input. When this discrete analog value is passing along the tapped delay line, it turns on each tap multiplier, so the instantaneous signal on the sensor is spatially sampled and scanned out at fixed time intervals corresponding to the clock frequency of the CCD shift register. After low pass filtering or sample and hold operation, a continuous time varying signal corresponding to the spatially varying signal is obtained.

By using an impulse of strength larger than one, $h(t) = AI(t)$, then h(t) will scan out the instantaneous incident signal present at the sensor elements, but with an output increased in amplitude by A. The increase in amplitude can be used to overcome noise, generated within the scanned array system.

This example is used only to show how the basic block of this system works.



a. OPTICAL SYSTEM



b. EQUIVALENT LINEAR SYSTEM

Figure 18 - FOURIER TRANSFORM

The emphasis on this system lies in its potential realizability in carrying out the spatial Fourier transform of the signal incident on the array. Spatial Fourier transforms play an important role in image data bandwidth reduction, in frequency beam forming, lensless imaging, and in other spatial processing operations[15].

An analogy from Fourier optics, outlined by H.Andrews, will help to understand the scanned array spatial Fourier transformation. Consider an optical system and its equivalent as in Fig 18. A monochromatic wave field at the input plane is convolved with a quadratic phase factor which is a function of the distance changed. Consequently, propagation of a wave field through a distance f is equivalent of convolution by a "chirp" function $\exp(j\pi(x^2+y^2)/\lambda f)$ where f is the focal length of the spherical lens. The positive spherical lens is equivalent to multiplication of the input wave by the same chirp function but with negative sign. In propagating to the output plane on the backside of the lens, the waveform undergoes another convolution with the same chirp rate as before, where the lens equation 1/f1 +1/f2 = 1/f must be satisfied. The wave field at the output plane is described mathematically by:

$$F(x,y) = f(x,y) * h1(x,y) \times \exp(-j\pi(x^2+y^2)/\lambda f) * h2(x,y).$$

Since the convolving scanned array executes a convolution of the sensor wave field with a given function h(t), the operation of a complete Fourier transform in one dimension consists of convolving spatially the input wave field with the chirp function h1(x), multiplying by chirp with negative sign, and finally another convolution with h2(x).

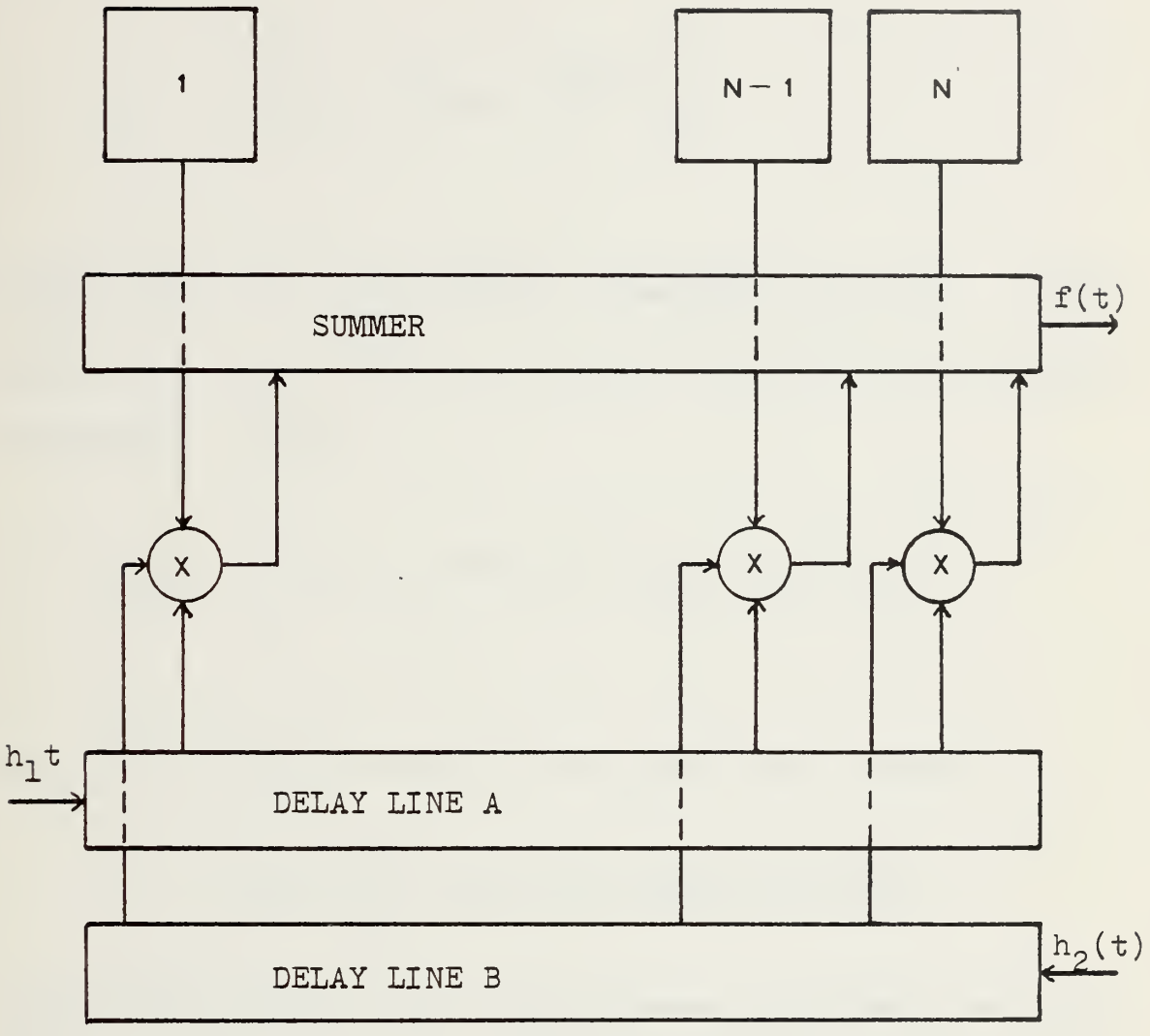


Figure 19 - INTER ARRAY FOURIER TRANSFORM

A system which implements this operation is shown in Fig 20. The expression for the Fourier transform in one dimension is:

$$F(t) = \int_{-\infty}^{\infty} f(x)\ e^{-j\pi tx}\ dx\ ,$$

where F(t) is the Fourier transform of f(x). After substituting the identity $tx=((t+x)^2-(t-x)^2)/4$ in the above expression, yields:

$$F(t) = \int_{-\infty}^{\infty} f(x)\ e^{-j\pi(t+x)^2/2}\ e^{j\pi(t-x)^2/2}\ dx\ .$$

The discrete time output of the system then becomes:

$$f(nT) = \sum_{i=0}^{N-1} f(iT)\,h1(nT-iT)\,h2(nT+iT-NT)\ ,$$

where f(nT) = f(x) is the instantaneous incident wave field, h1(t) is the scanning function applied to delay line A, h2(t) is the scanning function injected into delay line B, T is the delay from tap to tap, and NT is the total delay time of the delay line. By choosing $h1(t) = \exp(j\pi t^2/2)$ and $h2(t) = \exp(-j\pi(t+NT)^2/2)$, f(nT) becomes:

$$f(nT) = \sum_{i=0}^{N-1} f(iT)e^{-j\ (nT+iT)^2/2}\ e^{j\ (nT-iT)^2/2}\ ,$$

which is the Fourier transform of f(x); since f(1) corresponds to the signal of the first element in the array and for each shift of T seconds, the fixed distance between adjacent elements can be assigned, where the effective delay line propagation velocity v acts as a scaling factor. (vT = x1 , v2T = x2, ect).

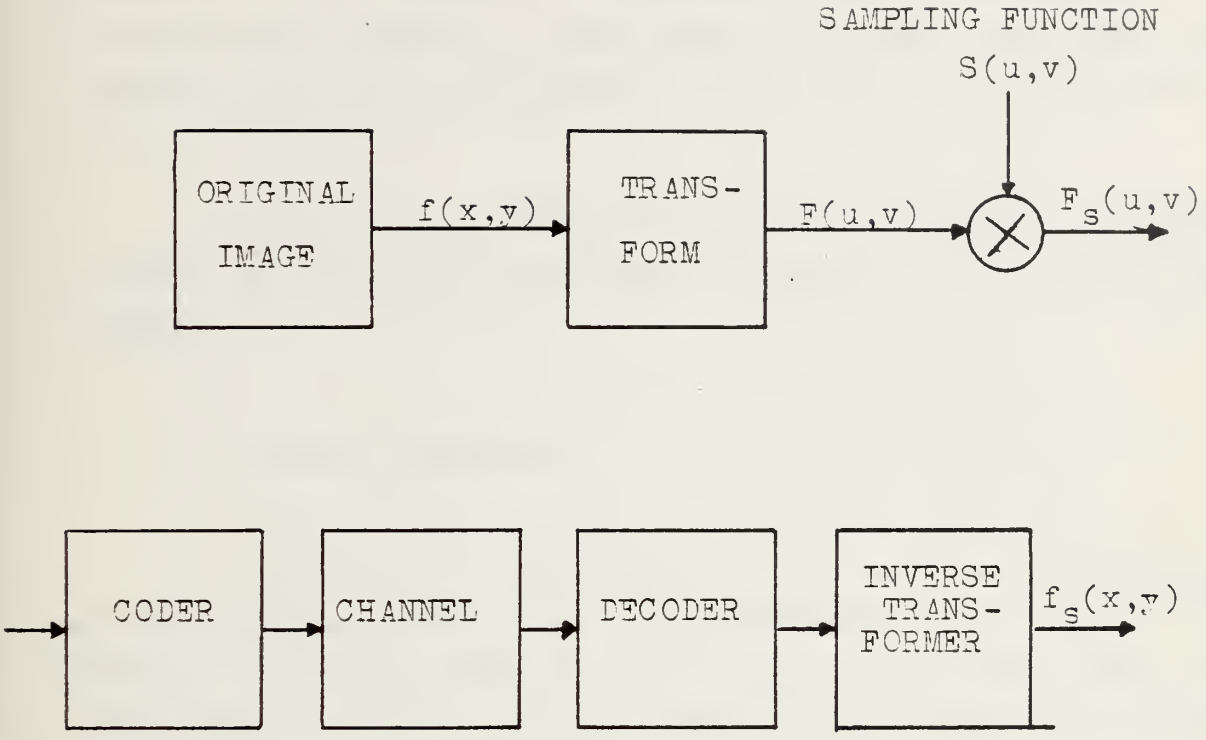
This concludes the discussion of signal processing in spatial domain. The last example has shown that when the convolution is carried out spatially, the output signal is transformed by the tapped delay line into the time domain.

Signal processing based on orthogonal transformations besides the Fourier transform will be highlighted in the next section.

D. PROCESSING IN TRANSFORM DOMAIN

1. Introduction

Transform coding techniques are mostly used to reduce redundancy in television image transmission. Several orthogonal or unitary transforms have been studied. Only a few, for which a high speed and easy to implement algorithm have been found, offer efficient way in real-time image coding. Since binary coded signals are the most suitable signalforms for transmission and simulation on digital computers, most of the transformations and sampling are done in the transform domain. For a system block diagram ,see Fig 20.



Possible Sampling Function	S(u,v)	Conditions
Checkerboard sampling	$\frac{1+(-1)^{u+v}}{2}$	odd samples=0
Random sampling	1 0	Prob.=p Prob.=1-p
Zonal sampling	1 0	u,v in sampl.region u,v not in s.region
Threshold sampling	1 0	if F(u,v) Thresh. if F(u,v) Thresh.

Figure 20 - TRANSFORM DOMAIN SAMPLING

There are no immediate applications of these transforms for IR focal plane processing. But several projects are going to consider these techniques for detecting and tracking satellites at high altitudes and tracking ballistic missiles after their initial booster burn.

Therefore, a brief summary over different transform methods applicable in real-time processing will close this chapter.

2. Fourier Transform

The Fourier transform of an image is the Fourier series representation of a two dimensional field [11]. To satisfy the periodicity condition, the image must be considered to be periodic horizontally and vertically. The advantage of the conjugate symmetry of the Fourier transform allows the use of only half the samples in the transform plane. Thus for an image containing N^2 elements, the transform has $2N^2$ elements, including both the magnitude and the phase of each transform element. But only N^2 are needed to preserve all the information. A mathematical expression for the Discrete Fourier Transform (DFT) is given by:

$$G_k = \sum_{n=0}^{N-1} e^{-i\pi 2nk/N} g_n \quad k = 0, 1, \ldots N-1 .$$

An example of this type of transform has been outlined previously in the spatial domain. A simple but useful

substitution of $2nk = n^2 - k^2 - (n-k)^2$ into the above expression, has led to an algorithm called Chirp-Z Transform (CZT).

3. The Chirp-Z Transform

A linear filter implementing this algorithm, using CCD or CTD as hardware building block for convolution, has been demonstrated for real-time computation [15]. Making the above mentioned substitution, the DFT becomes:

$$G_k = e^{-i\pi k^2/N} \sum_{n=0}^{N-1} e^{i\pi(n-k)^2/N} \, e^{-i\pi n^2/N} \, g_n \quad .$$

This expression suggested a three steps algorithm to perform this transform: a multiplication by a discrete chirp, a convolution with a discrete chirp of twice the length, and a postmultiplication by a discrete chirp. Compared to other transform methods, this algorithm is in the most advanced stage of hardware implementation. The reference function used in the pre-and post multiplication can be stored in a read only CCI-Memory, while the convolution is realized by a LSI charge transfer chip, and the multiplications are performed by linear IC multipliers.

A further extension of the DFT are two different types of cosine transform (DCT): an odd and an even DCT. The odd DCT extends the data block of length N to a length 2N-1, with the middle point as a center of even symmetry.

$$G_k = \sum_{n=-(N-1)}^{N-1} g_n \, e^{\frac{-i2\pi nk}{2N-1}} \quad \text{for } k = 0, 1, \ldots, N-1 \; .$$

The even DCT extends the length N data block to length 2N, with center of even symmetry at a point nearest the middle.

$$G_k = e^{\frac{-i\pi k}{2N}} \sum_{n=-N}^{N-1} g_n \, e^{\frac{-i2\pi nk}{2N}} \quad \text{for } k = 0, 1, \ldots, N-1 \; .$$

Both versions of DCT can be easily realized by using the real part of the chirp-Z transform algorithm.

VI. CONCLUSIONS

The interface circuit between a high resistance infrared detector and a SiCCD is studied. The detector resistance is in the order of one to ten megaohms which corresponds to typical cooled PbS and PbSe detectors. The CCD voltage gain is used to approach (accomplish) detector noise limited operation.

The following studies have been carried out:

1. The electrical operation of a two phase surface channel CCD with four input gates was measured and characterized by dc transfer characteristics. Three types of modes were found: one nonscuppering, inverting mode, two scuppering modes one inverting and the other noninverting. For the nonscuppering modes voltage gain ranges from 1 to 7 have been measured. A simple physical model based on surface potential equilibration and CCD geometry was developed to explain the gain mechanism.
2. The interface circuit is studied by a computer analysis program for three objectives:
   a. dc-coupling to minimize the fixed pattern variations of the detectors and their loads and to provide background suppression capability.
   b. providing a low pass transfer characteristic to bandlimit the noise in front of the CCD input.
   c. minimize the insertion loss.
3. CCD noise is measured which also included the study of the effect of aliasing due to the sampling process on the noise voltage measurements. Due to the large noise voltage of the output MOSFET on the CCD device used in this study, it was not possible to compare the noise of the different

input methods experimentally and to recommend the best method to accomplish the detector noise limited operating condition.

APPENDIX A

NOISE OF MOSFETS ON CCD CHIP

Noise sources in the low frequency region and the thermal noise for higher frequencies of MOSFETs on CCD chip are discussed in this appendix.

There are two noise contributions in the low frequency region:

1. Generation-recombination (GR) noise
2. Surface state or Flicker (1/f) noise.

For both, the surface and the buried channel MOSFETs, the generation-recombination centers in the depletion region under the gate are well known sources of low frequency noise [5,7].

For buried channel devices, the surface state effects can be neglected, and GR noise is dominant. However, at 77 degree Kelvin, it can be neglected, since the thermal time constants associated with these GR centers are extremely low.

In surface channel MOSFETS, Van der Ziel has shown that the surface state noise with its typical 1/f spectrum is the dominant low frequency noise. His experiments have demonstrated that the flicker noise is proportional to the surface state density Nss at the Fermi level.

Even though the exact frequency dependence is not clear at this time, it has been suggested that lower fast surface

state goes along with thinner oxides which agrees with the fact that the input-referred noise spectral density, V_n is proportional to the oxide thickness but varies inversely with the gate area. In order to minimize the spectral noise, it is helpful to maximize the area and minimize the fast surface state density and the oxide thickness. The maximum area is limited by the chip design, while the minimum oxide thickness will be limited by dielectric breakdown.Thus the fast surface state density Nss near the Fermi level is the most important parameter to lower the flicker noise.

Measured data of low frequency noise for p-channel on-chip MOSFETs are shown in Fig 21 and Fig 22. The test MOST transistors with larger W/L ratio of 20 are less noisy than the output MOST of the experimental CCD, which has a W/L ratio of 1. At the frequency of 100 Hz, the normalized noise is in the range from 1 to 5 V/ Hz.

The conclusion is, that the spectral noise level in the lower frequency region of the output MOSFET on the CCD used must be reduced by at least one order of magnitude.

For the "white" part in the noise spectrum, (not presented in measured data, due to the bandwidth of the RMS meter) the input noise at the gate results from the thermal noise in the channel.

The noise voltage is given by:

$$V_n = \left[\frac{2}{3}\, 4\, k\, T\, g_m^{-1}\right]^{1/2},\ \text{Volts Hz}^{-1/2},$$

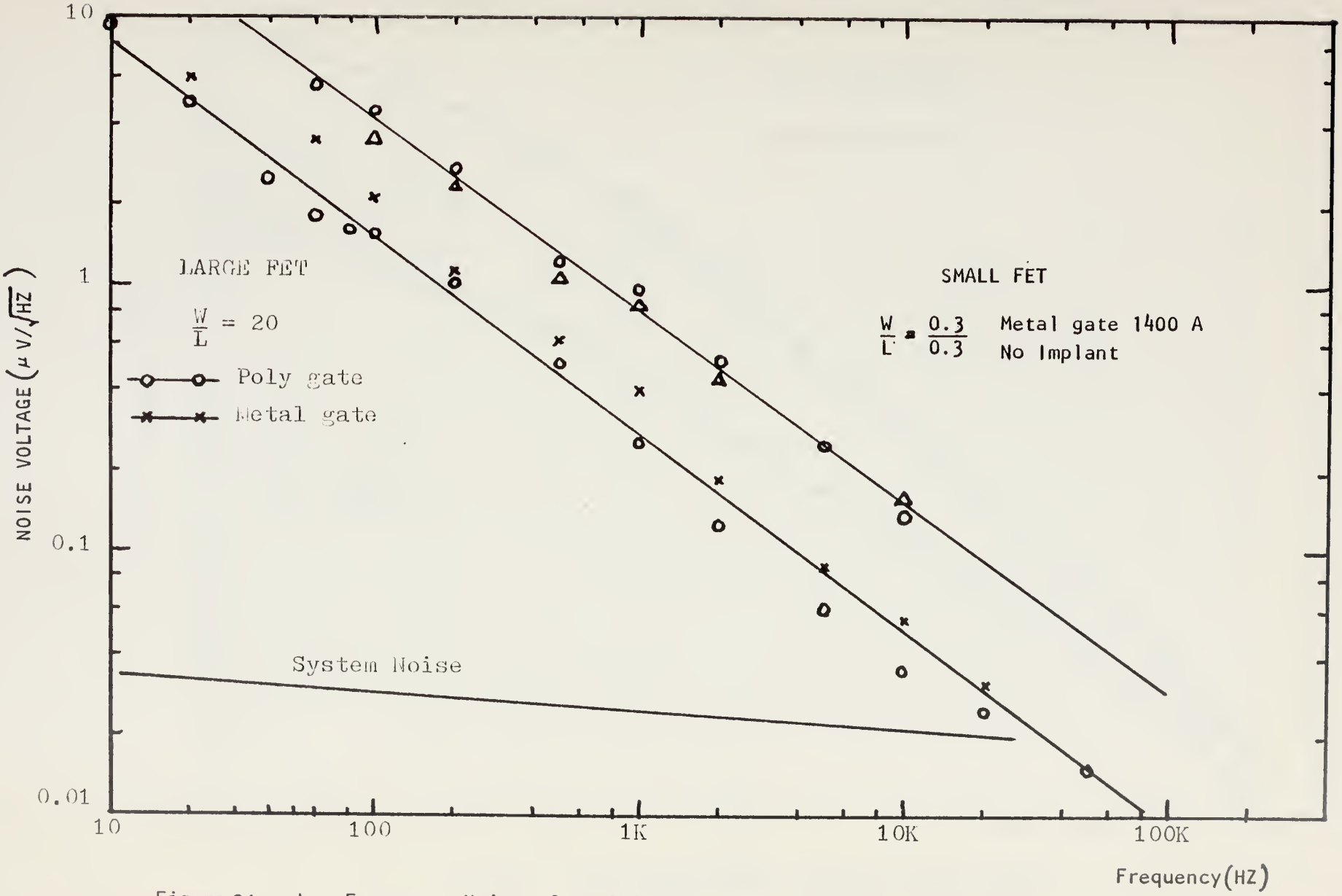


Figure 21 – Low Frequency Noise of on Chip MOSFET.

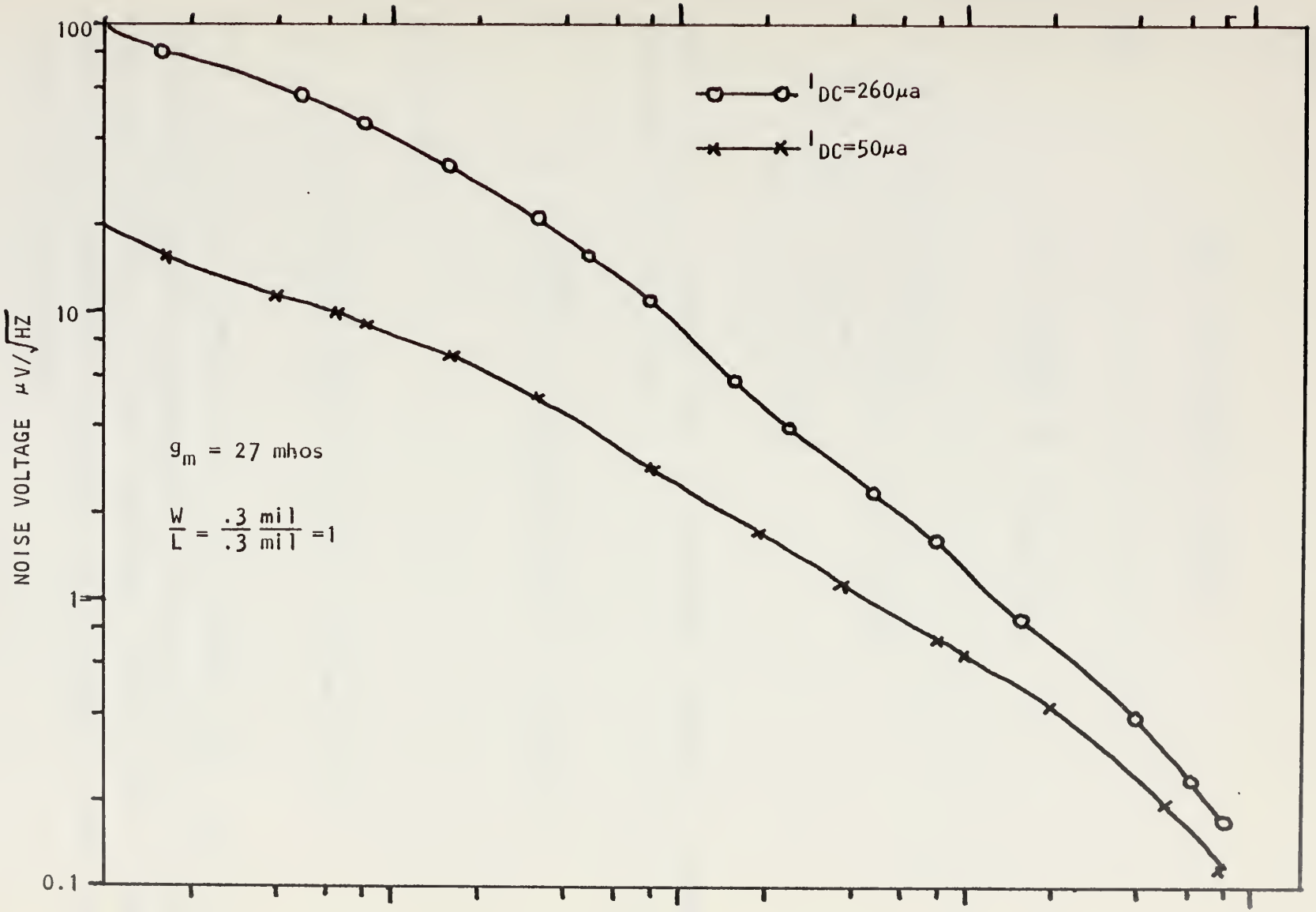


Fig.22 — CCD OUTPUT MOSFET SPECTRAL NOISE DENSITY

where

$$g_m = (2\beta I_{DC})^{1/2} \text{ , mhos ,}$$

and

$$\beta = \frac{\mu \epsilon_{ox}}{t_{ox}} \frac{W}{L} \text{ , mhos/Volt}$$

μ = carrier mobility
ϵ_{ox} = dielectric constant of the oxide
t_{ox} = oxide thickness
W = width of the channel
L = channel length

With typical numbers for a p-surface channel MOSFET, fabricated on a CCD chip:

$$\beta = \frac{\mu \epsilon_{ox}}{t_{ox}} \frac{W}{L} = \frac{150 \times 3.9 \times 8.85^{-14}}{10^{-5}} = 5.18 \times 10^{-6}.$$

At T=300°K

$$V_n = 1.85 \times 10^{-9} \left(\frac{W}{L}\right)^{-1/4} I_{DC}^{-1/4} \text{ , Volts Hz}^{-1/2}.$$

From this last equation it is obvious that when I_{DC} is limited by power considerations the ratio W/L is a very sensitive function of the required noise level. This theoretical calculation is valid in the region, where the thermal noise is dominant.

APPENDIX B

SAMPLED NOISE MEASUREMENTS

The fcld-tack cr aliasing effect of the sampling process cn noise measurements will be clarified in this appendix.

A. THEORY

Signal recovery through a sample and hcld circuit or scme kind cf hclding and low-pass filtering is widely used in signal prccessing, whether the processing is done digitally cr sampled analog.

The sampling or Nyquist theorem assures that a bandlimited signal x(t) with highest spectral frequency ccmponent f_M which is sampled periodically with sampling period $T_s \leq 1/2f_M$ can be uniquely reccnstructed by low pass filtering withcut distortion [16].

In cases, where the sampling frequency is low, the bandwidth cf noise generated within the circuit stretches out beycnd the Nyquist limit. The noise energy is fclded back intc the Nyquist bandwidth. In cases where the noise bandwidth is wider than twice the signal bandwidth, the fclding back cculd take place several times. This effect is shcwn in Fig 23.

Given a total available noise power P_n with a noise bandwidth BW, then the spectral noise voltage is:

$$V_n = [P_n \times BW^{-1}]^{1/2} \text{ , Volts per Root Hertz.}$$

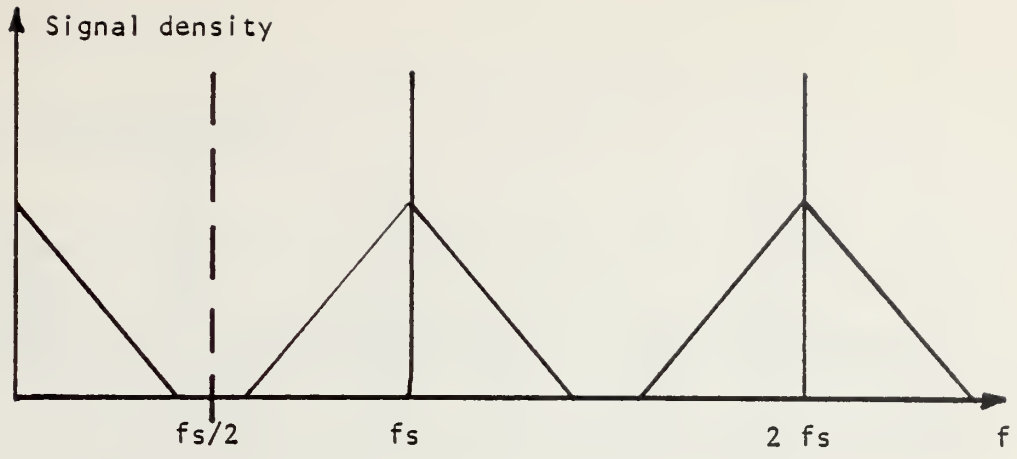
From Fig 24 we see that as long as the sampling rate is $f_s \leq 2BW$, a spectral noise voltage given above will be measured. However, when $f_s < 2BW$, the noise power within the Nyquist frequency and the spectral noise voltage will be increased due to aliasing. At $f_s = BW$, the noise power within the Nyquist range becomes:

$$P_r(f_s/2) = V_n^2(f_s/2) + V_n^2(f_s/2) \text{ watts .}$$

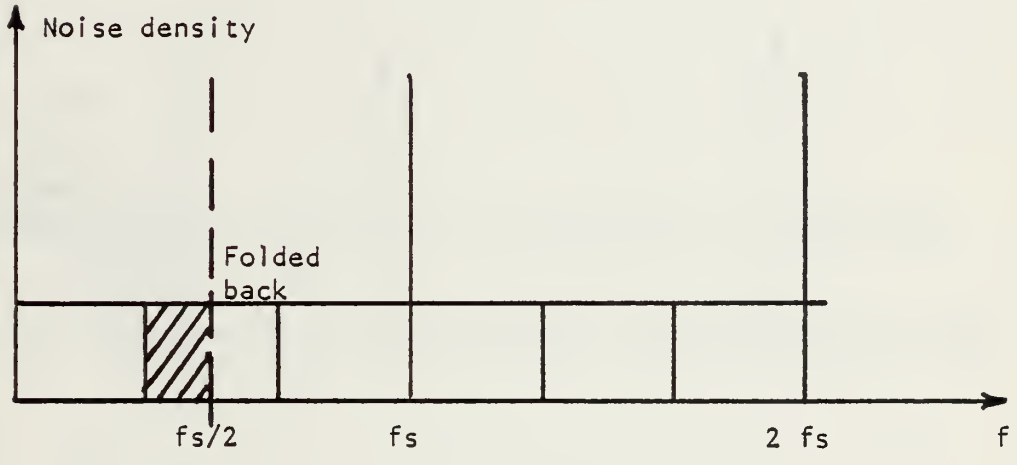
Even though the total available noise power did not change, the spectral noise voltage will be increased to

$$V_n = [P_n/f_s/2]^{1/2} \text{ , Volts per [Hz]}^{1/2}.$$

It depends on the inverse square root of the bandwidth $(f_s/2)$, resulting in an increase in spectral noise voltage.



sampled band limited signal



band limited noise

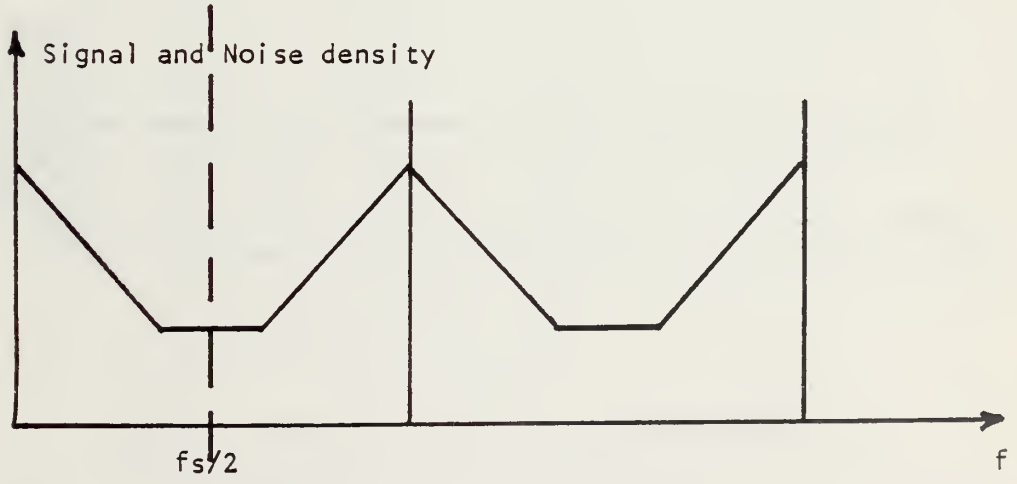


Figure 23 - INSTANTANEOUSLY SAMPLED SIGNAL AND NCISE

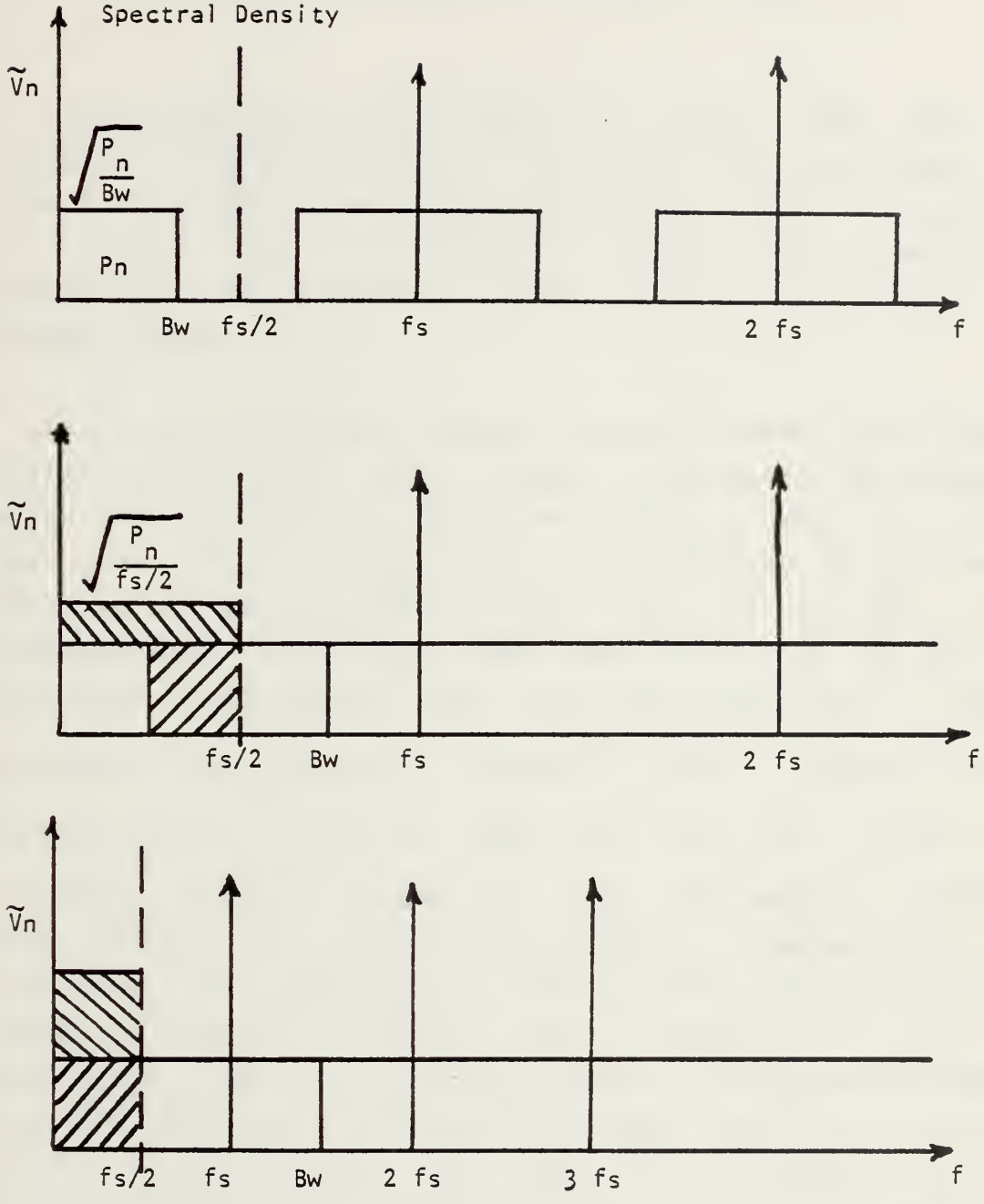


Fig. 24 — FOLDING BACK EFFECT BY UNDER SAMPLING

B. EXPERIMENTAL VERIFICATION OF SAMPLED NOISE

An experimental setup, shown in Fig 25, was used to verify the aliasing effect of noise discussed previously. A noise source (GR 1390-B Random Noise Generator) is applied to a sample and hold circuit (Analog Device SHA-2) and measured by a PAR Lock-In Amplifier (LIA) used in its RMS Voltmeter mode.

In Fig 26, measured spectral noise voltages for various sampling frequencies are shown. For sampling frequencies larger than 250 KHz, the aperture effect cannot be seen, since the LIA is bandlimited to 250 KHz. The GR noise generator provides two ENBW of 500 KHz and 20 KHz. The experimentally determined ENBW was found to be 720 KHz and 50.25 KHz. These datas were used to calculate a total available noise power of 0.784×10^{-6} watt for ENBW of 50.25 KHz and 2.88×10^{-6} watt for ENBW of 720 KHz. Using the previously derived expression, the theoretical spectral noise voltage for different sampling frequencies was calculated. The experimental data and the theoretical noise voltage vs sampling frequency are presented on Fig. 27. This graph clearly demonstrates that in every measurement, where a sample and hold circuit is used and no low pass filter can be applied in front of the sample and hold circuit, the measured spectral noise voltage is strongly dependent on the sampling frequency.

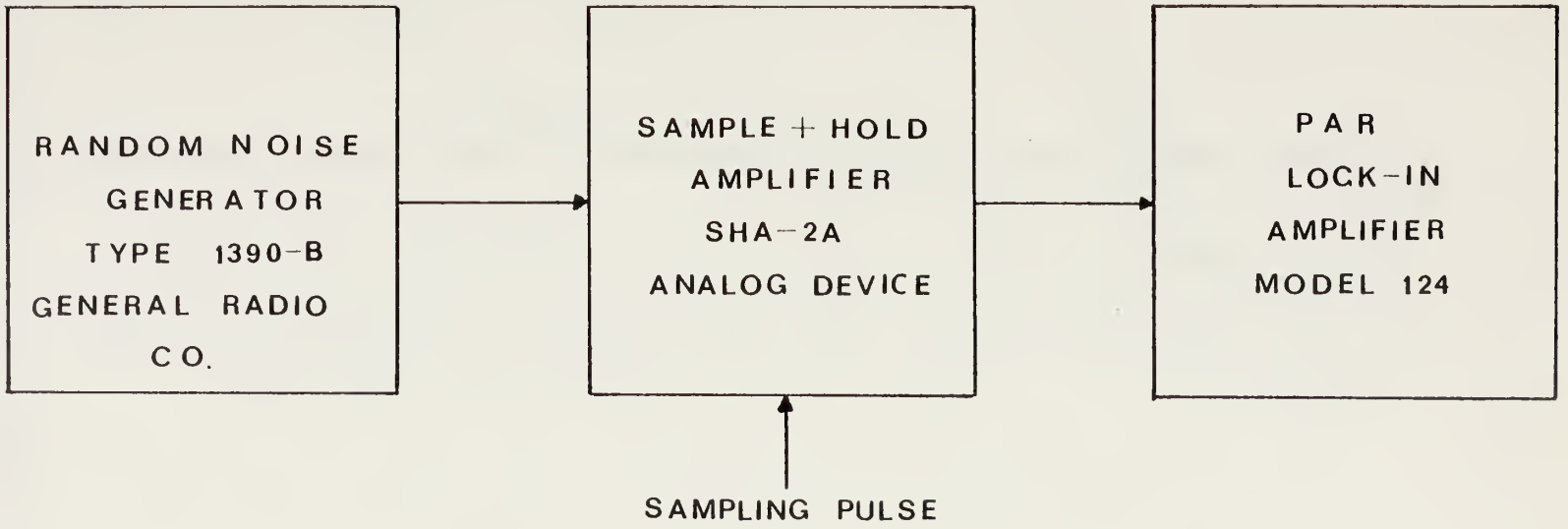


Figure 25 - EXPERIMENTAL SET UP FOR SAMPLED NOISE.

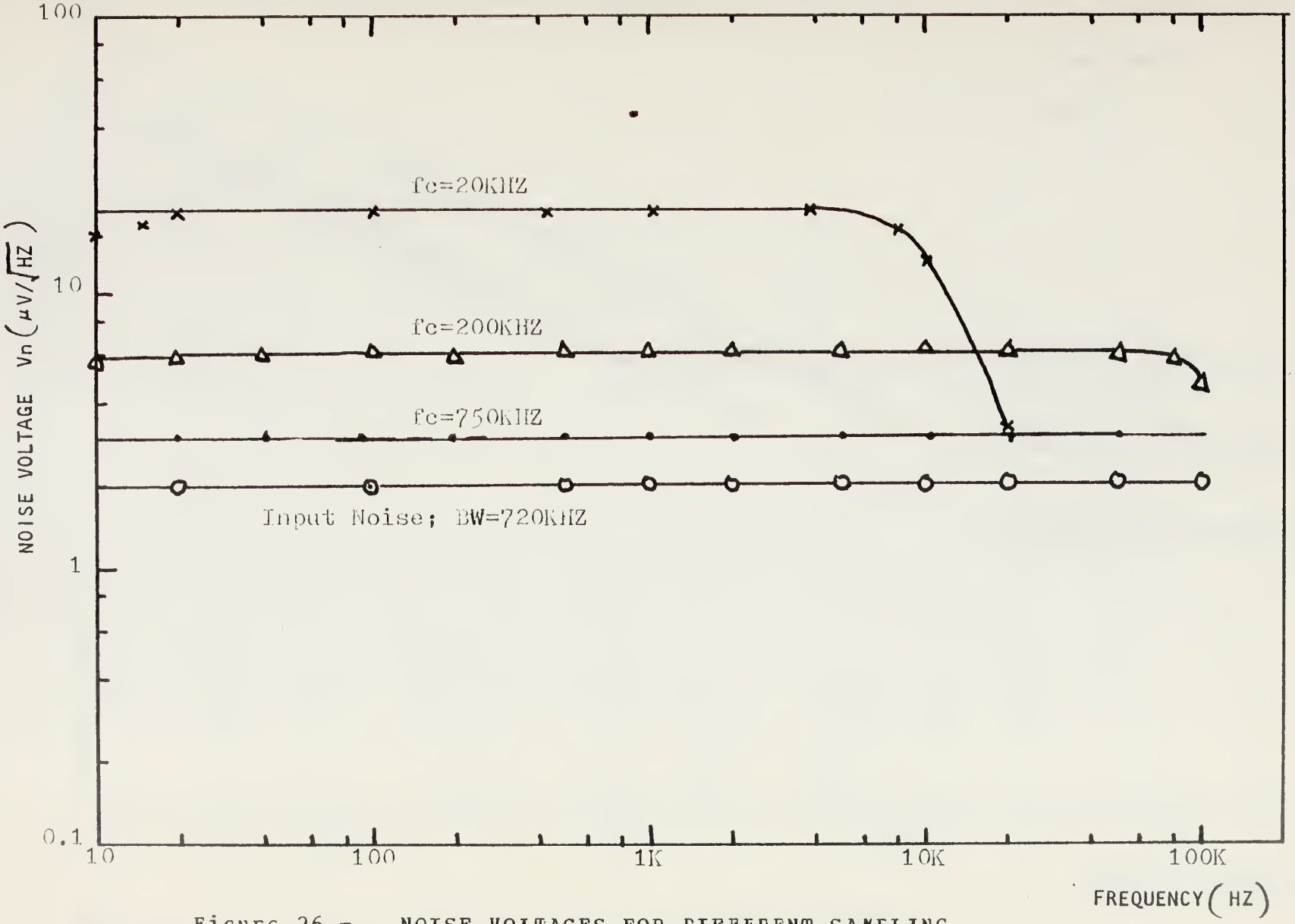


Figure 26 - NOISE VOLTAGES FOR DIFFERENT SAMPLING FREQUENCIES

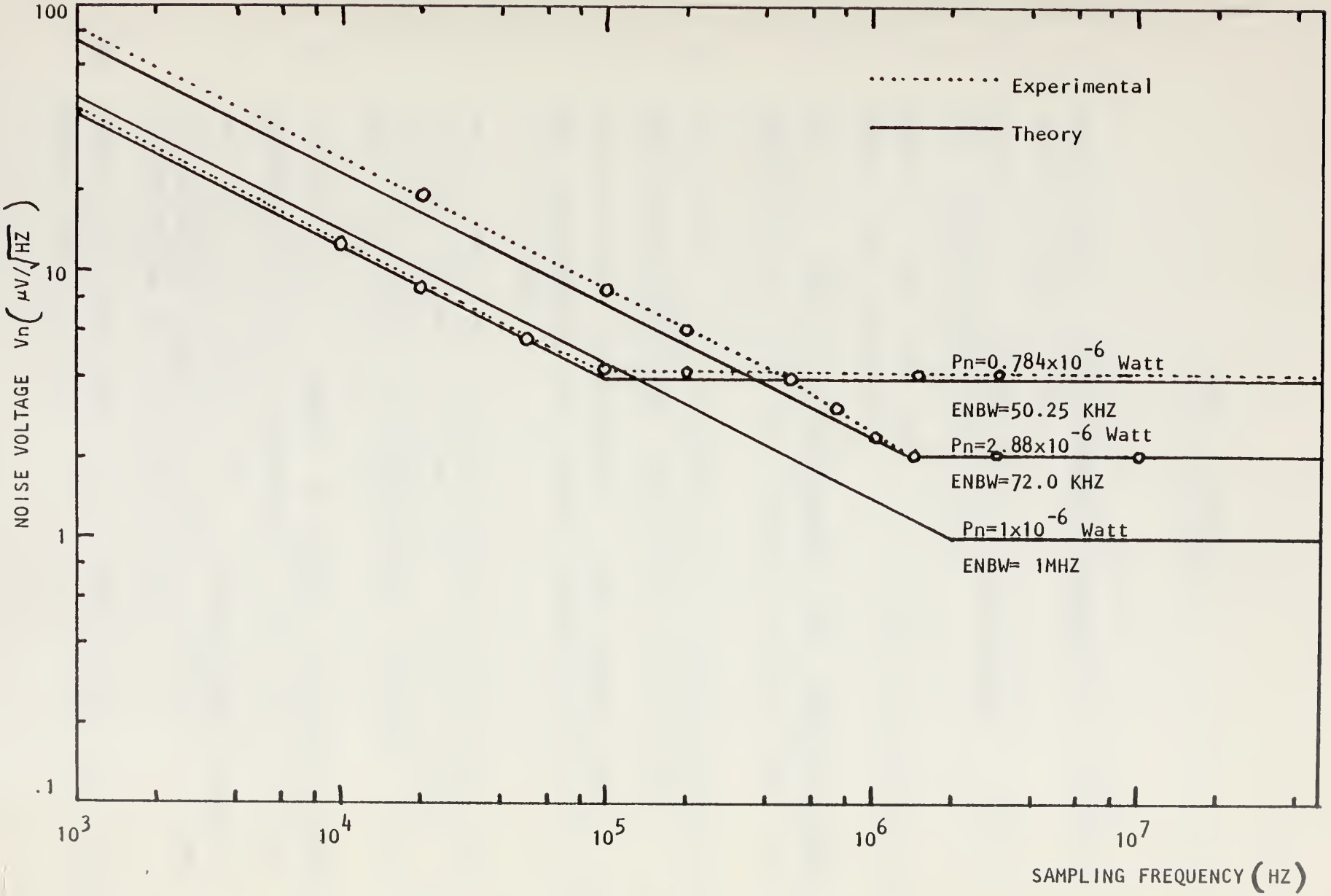


Figure 27 - SPECTRAL NOISE VOLTAGE VS SAMPLING FREQUENCY

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